

Replacing the Cypress CY14B256LA-SZ45 nvSRAM with Everspin MR256A08BxSO35 MRAM

GENERAL CONSIDERATIONS for REPLACING nvSRAM with MRAM

Every write with an MRAM is instantly non-volatile for at least 20 years. There is no transfer of data from a volatile to a non-volatile memory cell, no external capacitors or back up batteries. The elimination of external components, highly reliable data retention, and 35ns SRAM compatible READ/WRITE Access times makes the Everspin MRAM a viable candidate for replacing the Cypress CY14B256LA-SZ45 nvSRAM without compromising system performance.

EVERSPIN MRAM MEMORY

Everspin is the global leader in commercially viable MRAM technology and Everspin MRAM products are present in hundreds of applications demanding high-speed, reliable, non-volatile memory.

MR256A08B COMPARISON TO CY14B256LA

The Everspin MRAM solution provides:

- Always non-volatile. No unreliable capacitor dependent backup cycles
- No V_{CAP} or V_{BATT} required
- Immediate (<1ns) Power-off with no loss of data
- No complex Software STORE/RECALL routines
- Fast Start-up time (2ms vs. 20ms)
- Unlimited Read and Write cycles - no Wear-out concerns
- 20-Year Data Retention with No Cycling Dependence
- Fewer components means smaller design footprint and lower total BOM cost
- Directly replaces the Cypress nvSRAM

COMPATIBILITY

The Everspin MR256A08BxSO35 (32-SOIC) MRAM memory is pin and timing compatible with the Cypress CY14B256LA-SZ45 nvSRAM.

TIMING COMPATIBILITY

Both Everspin MRAM and nvSRAM have standard, compatible asynchronous SRAM timing. The MRAM however, retains data even at power off for an indefinite period of time and over temperature cycling. With a 35 ns read/write cycle time, the MRAM is compatible with similar nvSRAM speed grade options.

It is important to note that the Everspin MR256A08Bxxx35 device requires a minimum of 12ns hold time from Write Enable (and Chip Enable) high to Address invalid (Please see

T_{WHAX} and T_{EHAX} in the MR256A08B data sheet available [here](#).) Most microprocessors can accommodate this Hold time.

PIN COMPATIBILITY

- 256Kb organized in the 32Kx8 configuration
- 3.3 volt nominal operation
- Standard SRAM parallel address pins (A0-14)
- Standard byte-wide, bidirectional data pins (DQ0-7)
- Standard control signals (/E, /W, /G)

The MR256A08B does not require an external capacitor and other associated passive components required by the CY14B256LA-SZ45 device.

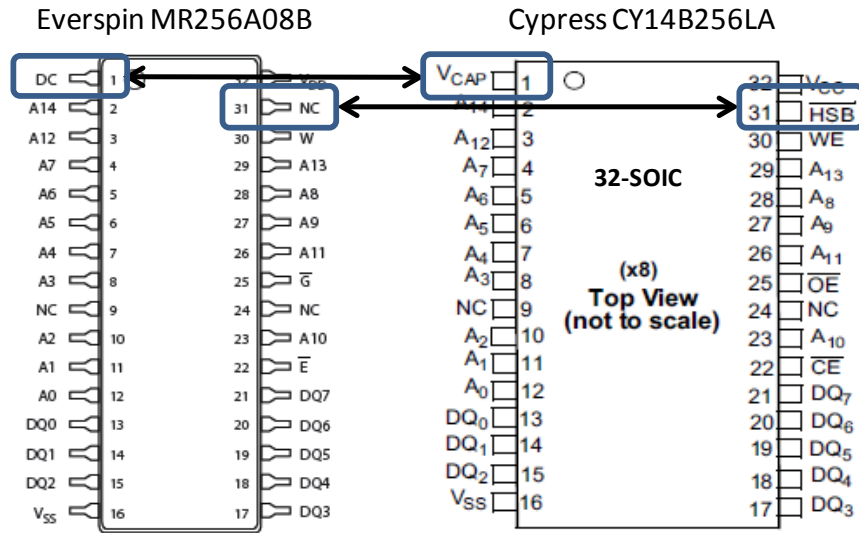
The primary differences between the Cypress and Everspin devices are the two pins on the nvSRAM: V_{CAP} and /HSB. These pins are used to support the nvSRAM backup cycle and are not required for operation of the MRAM.

V_{CAP} pin

A capacitor is required on the V_{CAP} pin (Pin 1 of the SOIC) on nvSRAM devices. Everspin assigns a “Do not connect” (DC) to the corresponding pin on the MRAM. When replacing the Cypress nvSRAM with the Everspin MRAM, it is recommended that this pin be either left floating or pulled to V_{SS} . The Vcap capacitor should not be used with the Everspin MRAM.

/HSB pin

The /HSB pin of the nvSRAM (Pin 31 of the SOIC) is used to either initiate a Hardware Store or indicate a Hardware Store is in process. Because this pin is not connected (NC) on the MRAM, a Host processor should not expect the MRAM to drive this I/O to a particular voltage level.



Pin Function Comparison SOIC Package

Figure 1: Pin function comparison between MRAM and nvSRAM, 32 pin SOIC Package

PIN #	Everspin	Cypress	Everspin connection	Everspin Comments
1	DC	VCap	Do not connect	Must be kept at a Steady State. Prefer floating or tied to Vss to minimize current draw. Suggest do not connect nvSRAM Capacitor
9	NC	NC	Not connected to die	Prefer to float but may be tied to VIH or VIL
24	NC	NC	Not connected to die	Prefer to float but may be tied to VIH or VIL
31	NC	HSB_	Not connected to die	Do not expect this I/O to be pulled low

Table2: Pin function comparison between MRAM and nvSRAM, 32 pin SOIC package

OTHER REPLACEMENT DESIGN CONSIDERATIONS

HSB SOFTWARE

Due to its persistence, there is no power monitoring requirement for the Everspin MRAM as is the case with the nvSRAM. Hence initiating or monitoring Hardware Stores, Re-stores and associated software routines are unnecessary and can be eliminated.

SIMPLIFIED POWER CYCLING

When power is removed from the MRAM, data remain valid over 20 years' time and across the temperature range. This feature, unique to MRAM, allows for Duty Cycle Power control enabling the user to reduce their overall power consumption without the concern of wear-out.

MRAM requires control signals /E and /W to track the power supply during power-up and be held high for a 2 ms start-up period, a much shorter power-up requirement than the nvSRAM. When power fails, the Everspin MRAM simply inhibits write operations and no special power down timing considerations are needed since data is always non-volatile.

The nvSRAM device requires the /WE signal to track the power supply during power-up and be held high during the power-up recall period of 20 ms. The nvSRAM must sense the power failure, decouple the power supply from its backup capacitor, wait for any SRAM operations to complete, and then perform a parallel write to the EEPROM storage element during the 8 ms period after power has failed. This sequence is complicated by the fact that power falls at various ramp rates and in some cases bounces above and below the power supply threshold (brown outs) in rapid succession. Thus raising concerns about reliability of the backup storage cycle under all system power conditions including some that cannot easily be simulated or tested.

Everspin MRAM supports unlimited read, write, and power cycles. There are no wear-out concerns with MR256A08B.

POWER-UP SEQUENCING

Both MRAM and nvSRAM will operate from a standard +3.3 volt power supply with +/-10% power supply range. Both MRAM and nvSRAM have similar standby and active operating currents, however, the "Start-up" time for the MRAM is 2ms vs. 20ms for the nvSRAM. Proper decoupling capacitors should be used to assure reliable operation.

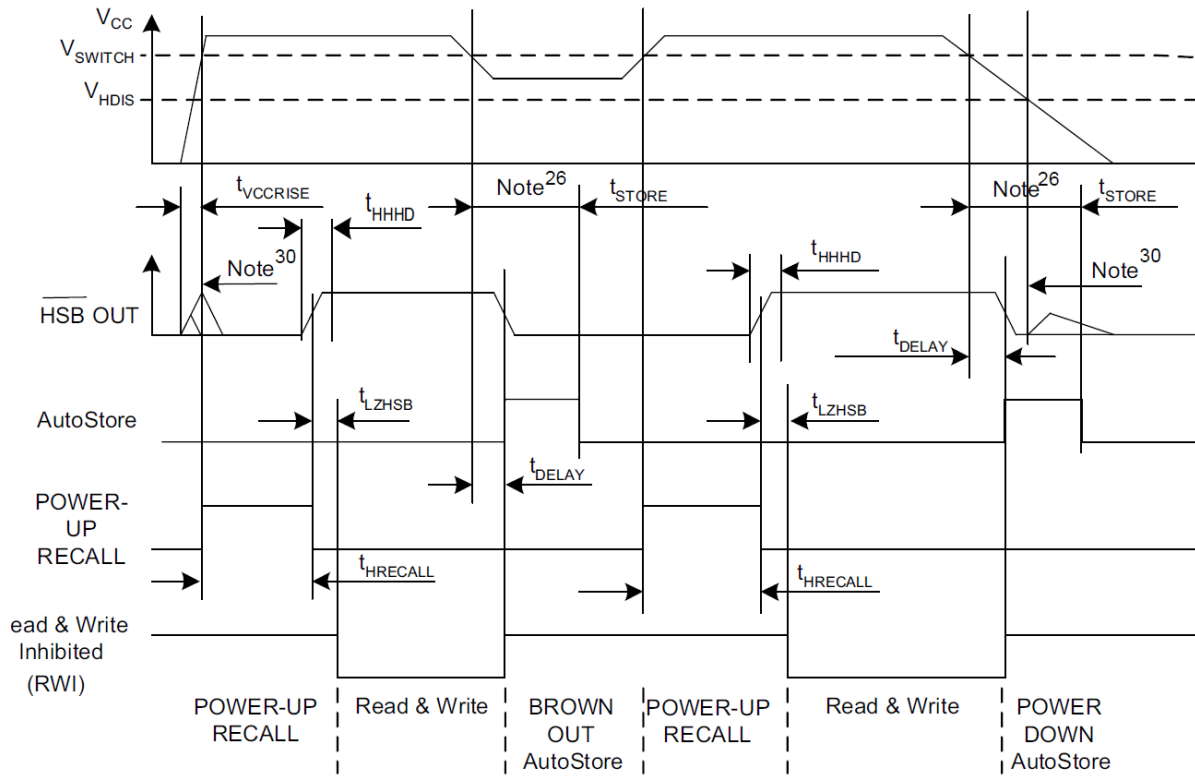


Figure 2: nvSRAM Power Up RECALL Timing

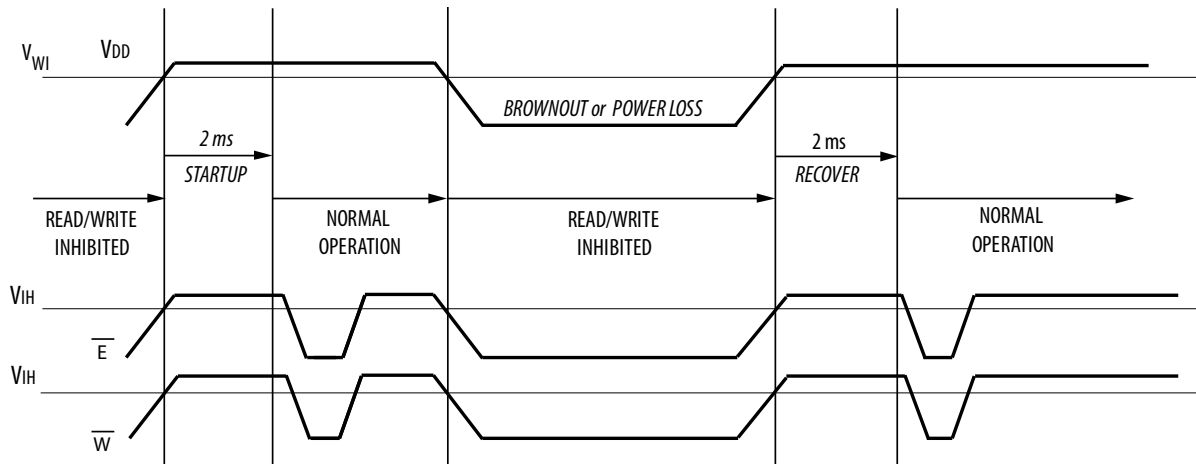


Figure 3: MRAM Power Down (Brownout) and Power Up Timing

RELIABILITY CONSIDERATIONS FOR COMPARISON

CY14B256LA uses conventional trapped charge technology for non-volatile storage. Data can leak away as wear-out results from temperature and excessive write cycles. Engineers must carefully design systems using nvSRAM to avoid exceeding the non-volatile write limitation of 1 million store cycles.

Everspin MRAM will provide the most cost effective non-volatile RAM solution. The nvSRAM is constructed by combining a standard 6-transistor SRAM with a non-volatile EEPROM storage element in every cell. The total cell complexity is 12-transistors. MR256A08B is built using a much simpler 1-transistor, 1-magnetic tunnel junction cell. The simple Everspin MRAM cell leads to improved manufacturing efficiency and increased reliability.

The reliability of an nvSRAM is dependent upon not only the memory chip but also the quality of the external V_{CAP} capacitor. Careful capacitor selection is necessary to assure reliable power sequencing.

MRAM uses magnetic tunnel junction technology for non-volatile storage. Data does not leak away at high temperature and there is no wear-out mechanism to limit the number of read, write, or power cycles in this technology. Data retention is better than 20 years at 125 °C.

OTHER PACKAGES

In addition to 32-pin SOIC and 44-pin TSOP2 packages, the Everspin 256Kb MRAM MR256A08B is available in an 8mm x 8mm FBGA package.

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Replacing the Cypress CY14B256LA nvSRAM with Everspin's MR256A08B MRAM

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