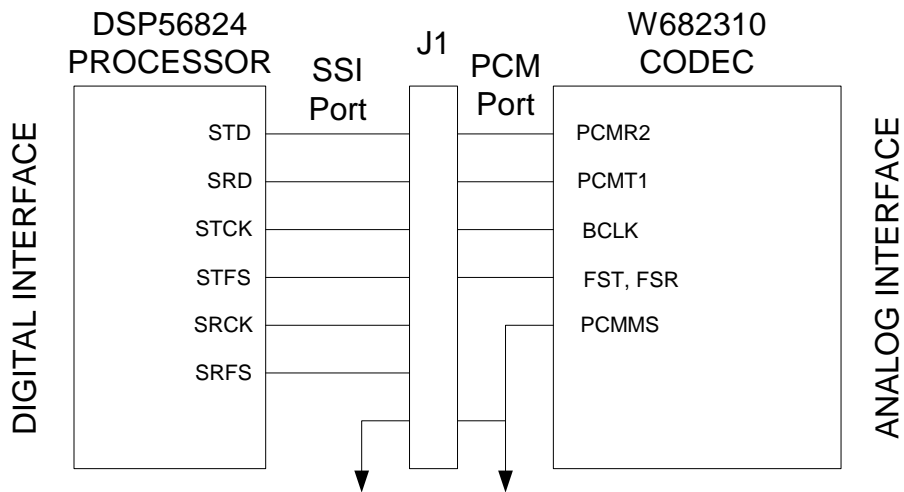


Interfacing the Nuvoton W682310 with Freescale DSP Processor through the Synchronous Serial Interface

Block Diagram of the SSI CODEC Interface



DSP Signal	CODEC Pin #	CODEC Signal	PCM Function
STD/PC8	9	PCMR2	Receive Data
SRD/PC9	11	PCMT1	Transmit Data
STCK/PC10	14	BCLK	PCM T/R bit clock
STFS/PC11	8,13	FSR/FST	8 kHz Frame Sync
SRCK/PC12	N/A		
SRFS/PC13	N/A		

This example uses a Freescale DSP56824 Digital Signal Processor. It has a two channel Analog Front End. The AFE is the Nuvoton W682310 CODEC. Using the Synchronous Serial Interface the processor can provide the timing signals to the CODEC PCM interface. It is important to decide

where the synchronization is coming from, either the DSP or externally. When the DSP provides the timing, a specific crystal frequency is chosen that will allow easy development of the PCM signals. For one DSP processor the following table covered three common telephony bit rates:

Bit Rate (BPS)	Crystal Frequency
1.536 MHz	36.864 MHz
1.544 MHz	37.056 MHz
2.048 MHz	32.678 MHz

By using its various dividers and counters the DSP can develop the proper PCM bit rate and the 8 kHz Frame Rate.

In this illustration the W682310 is operating in the Serial Mode. It is providing Channel 1 data in the first 8 bits after the Frame Sync. Channel 2 data follows in the next 8 bits. This reduces the number of data lines between the DSP and the CODEC. If the CODEC was operating in the Parallel Mode it would take more data lines.

The CODEC can be powered down when not needed. This can be done by using the SSI in the "On-Demand" mode. The Nuvoton CODEC will automatically power down if either the BCLK or FST/FSR signals are held constant at ONE or ZERO. In this state all the analog stages of the CODEC (except the internal reference voltage) are powered down. This greatly reduces power consumption. Note that when this mode is used, the internal PLL will take 2 to 10 milliseconds to lock upon clock resumption. In addition to the PLL lock time, the analog outputs will be set to internal signal ground for 1 millisecond. This is to avoid glitches at power up. During this power up delay the digital outputs will remain at high impedance.

An important piece of information to remember is that telephony CODECs expect and produce their data MSB (Sign Bit) first. It is nice when the DSP can have bidirectional input registers. This allows using the data in either sequence within the processor. Using the CODEC with a DSP processor, the PCM signal can be even further compressed (reduced) from the 64 KHz G.711 data rate to slower rates for other, more recent standards.

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