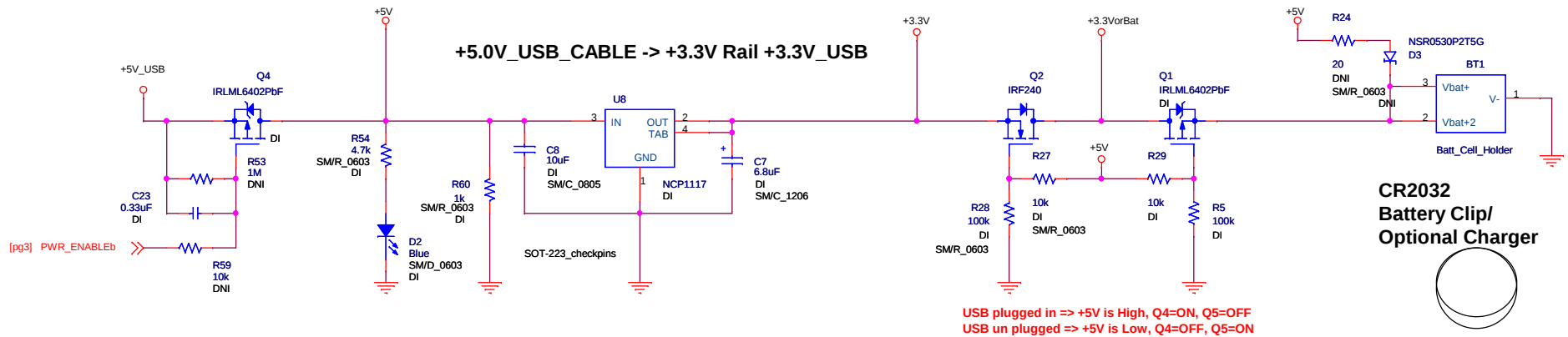
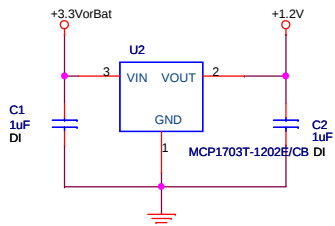
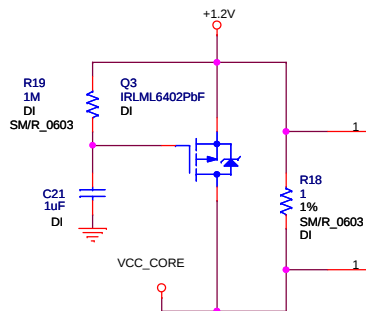




+3.3V or Bat -> +1.2V Rail

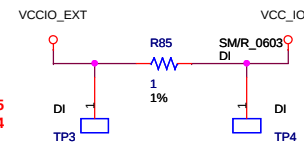


Core Current



To U9 sense for current
 Thin signal traces or non load bearing copper pour
 Direct path from R35 to U7

I/O Current



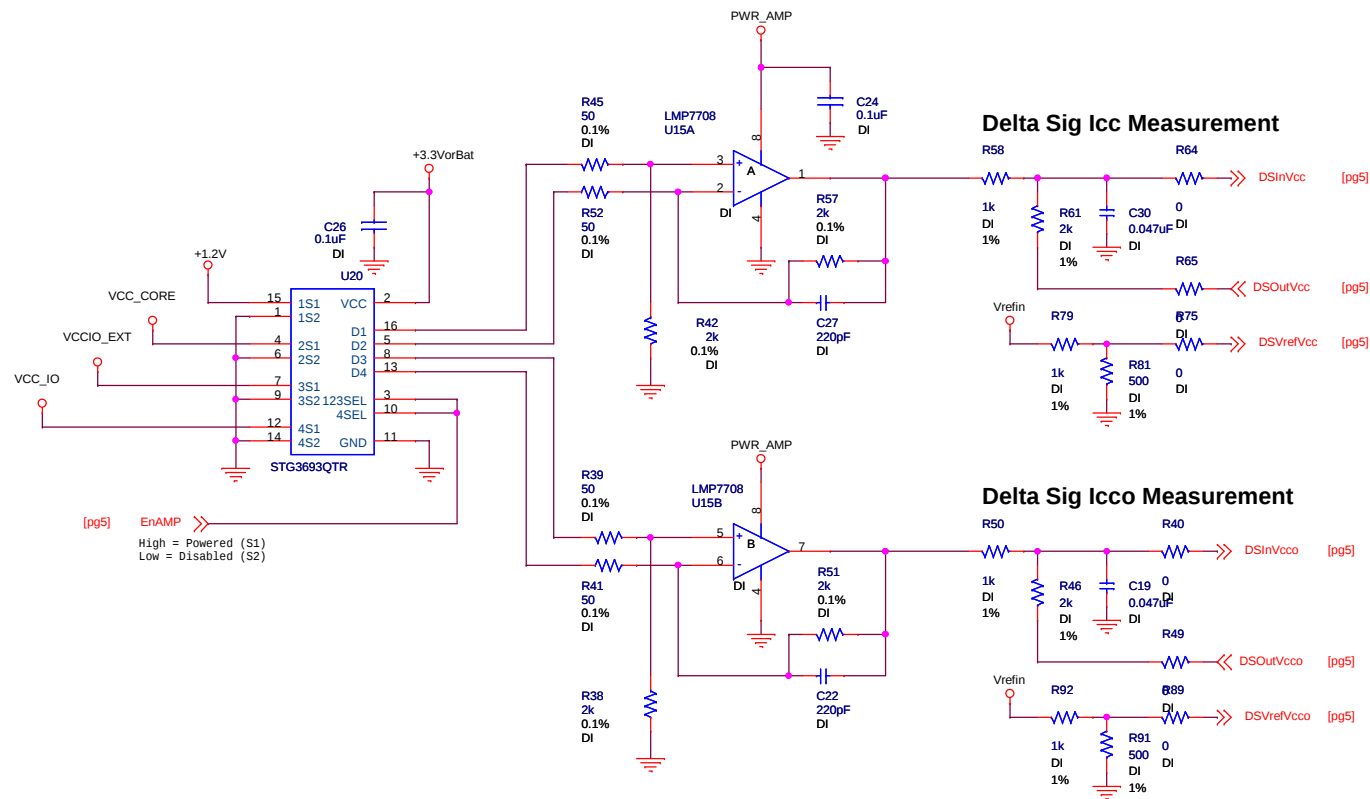
To U9 sense for current
 Thin signal traces
 Direct path from R34 to U7



Lattice Semiconductor Applications
 Email: techsupport@latticesemi.com
 Phone (503) 269-8001 -or- (800) LATTICE

Title
 USB 5V, XO Power Rails 3.0V Batt, 1.2V Rail and Current Monitors

Size B	Project MACHXO2 Pico Board	Schematic Rev A
Date: Friday, March 4, 2011	Board Rev E	Sheet 1 of 6

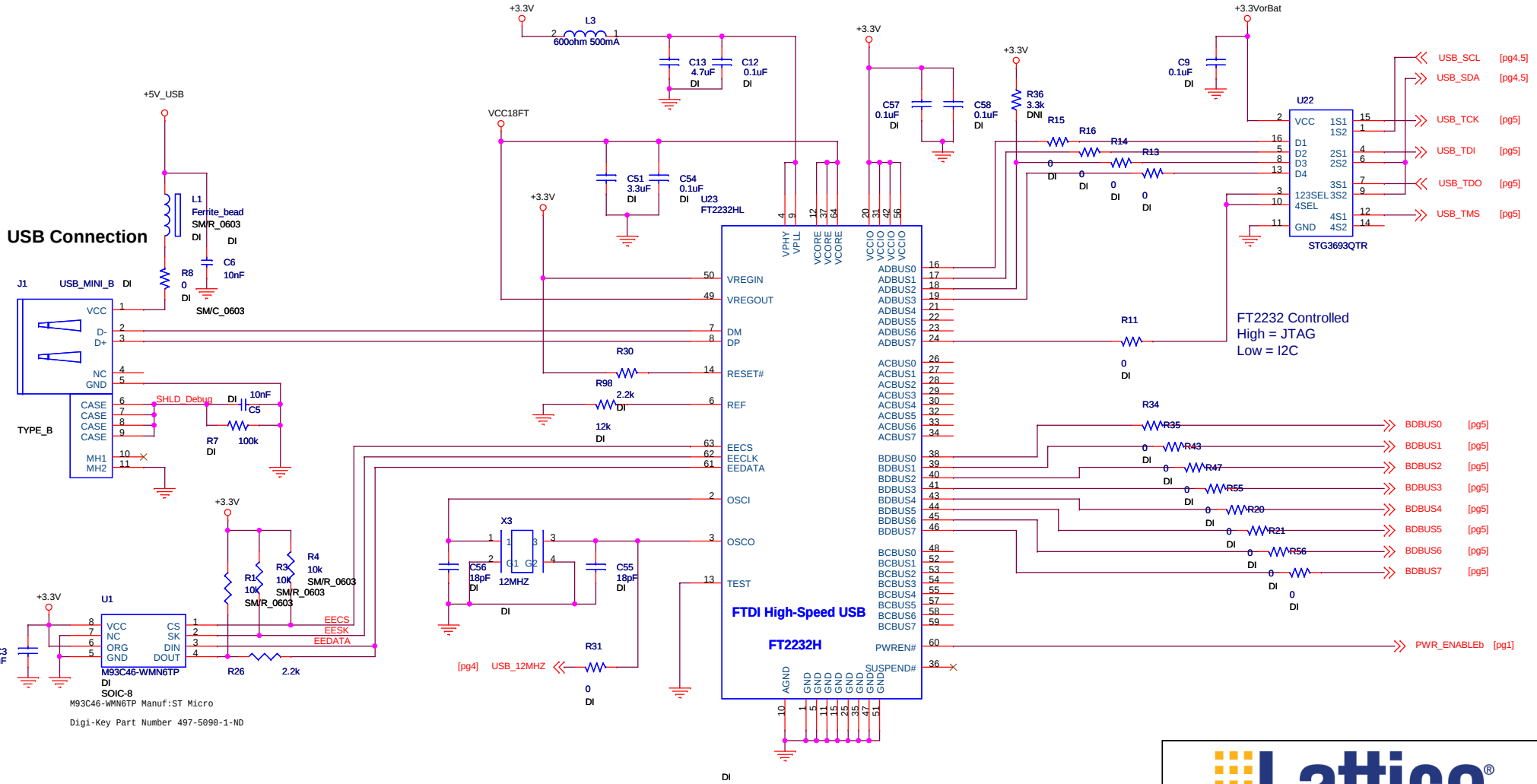


Lattice Semiconductor Applications
Email: techsupport@latticesemi.com
Phone (503) 268-8001 -or- (800) LATTICE

Title
Current Sense Amplifiers, Power Enable Mux

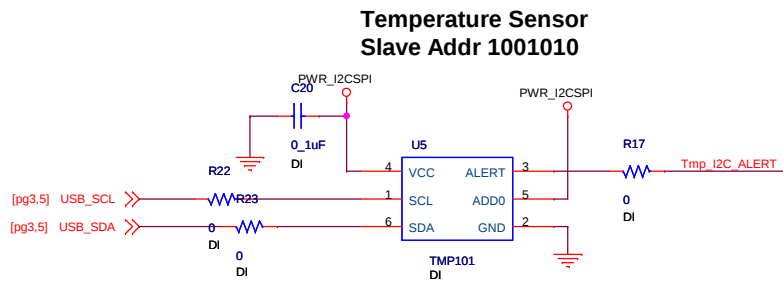
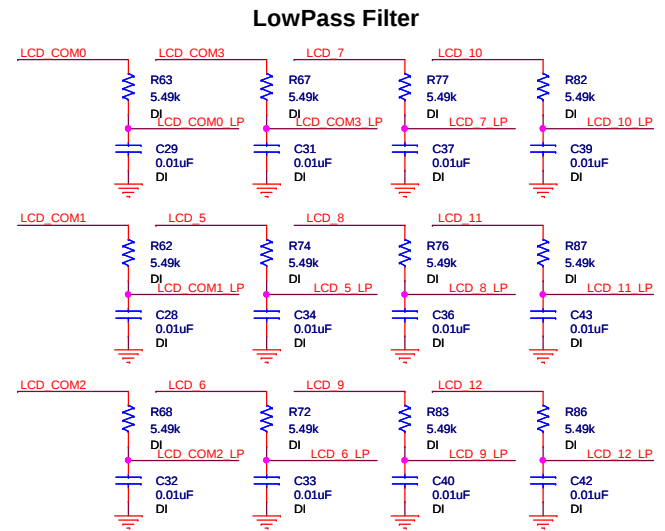
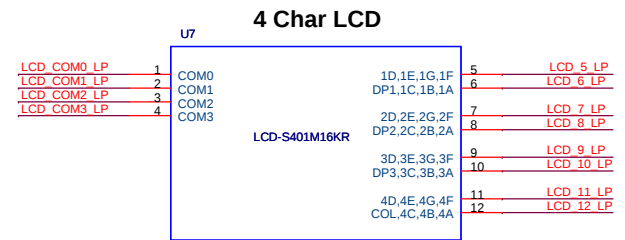
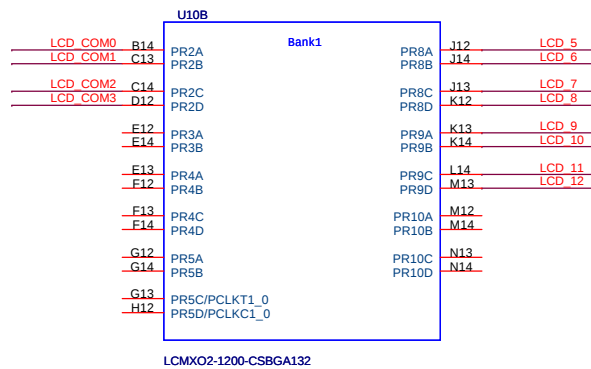
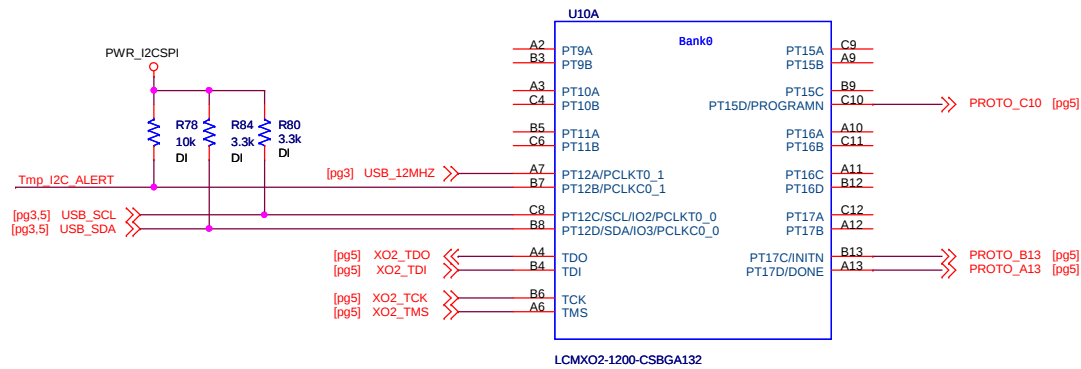
Size B	Project MACHXO2 Pico Board	Schematic Rev A
Date: Friday, March 4, 2011	Board Rev E	Sheet 2 of 6

USB Connection



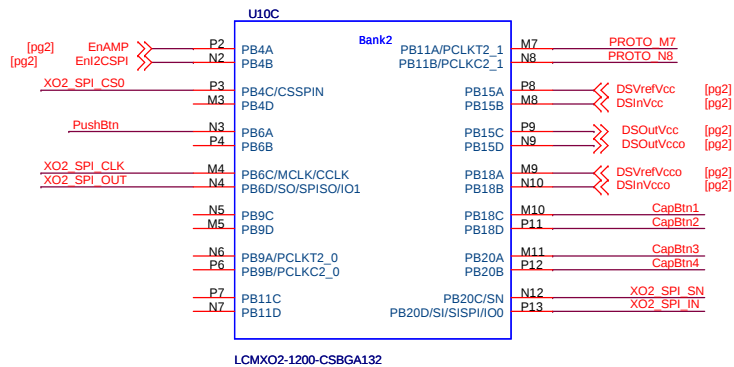
Lattice Semiconductor Applications
Email: techsupport@latticesemi.com
Phone (503) 268-8001 -or- (800) LATTICE

Title		
USB to JTAG and I2C for the XO2		
Size	Project	Schematic Rev
B	MACHXO2 Pico Board	A
Date:	Friday, March 4, 2011	Board Rev
		E
	Sheet	3 of 6

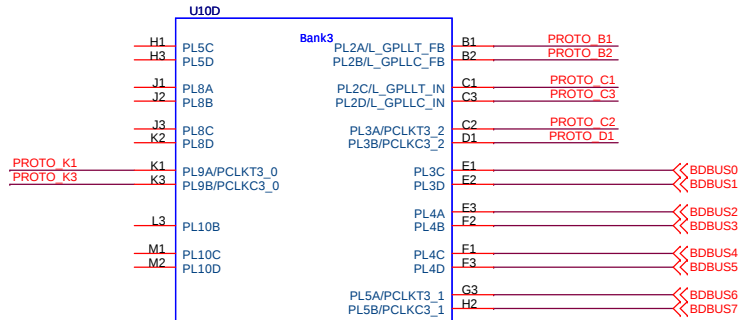


Lattice Semiconductor Applications
Email: techsupport@latticesemi.com
Phone (503) 268-8001 -or- (800) LATTICE

Title		
XO2 Bank 0-1, LCD, I2C Temp		
Size B	Project MACHXO2 Pico Board	Schematic Rev A
Date: Friday, March 4, 2011	Board Rev E	Sheet 4 of 6

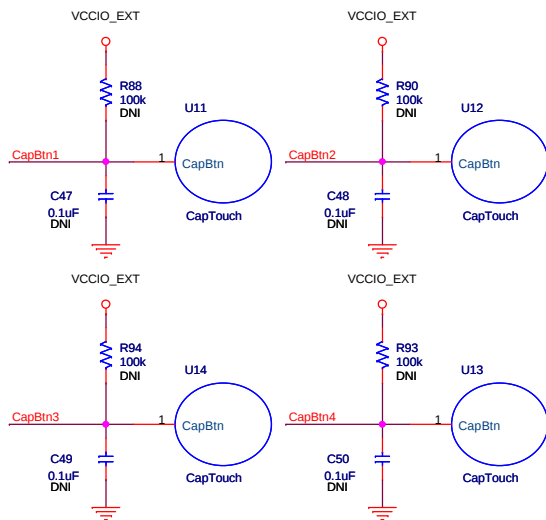


LCMXO2-1200-CSBGA132

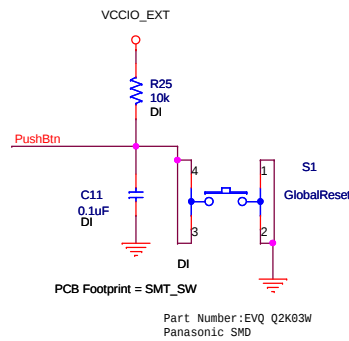


LCMXO2-1200-CSBGA132

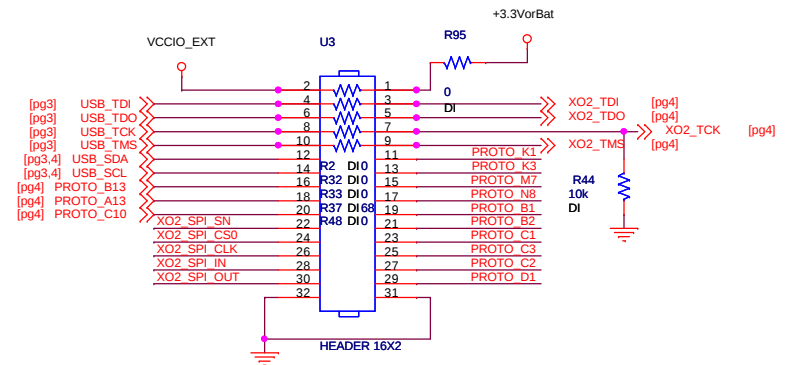
Capacitive Touch Pads



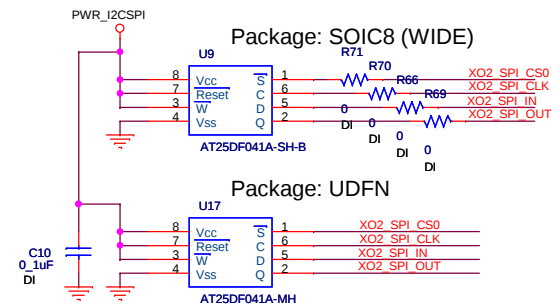
GSR/Wake from Standby



Header



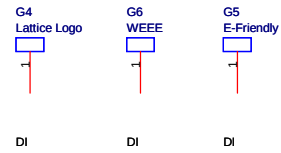
4MBit SPI



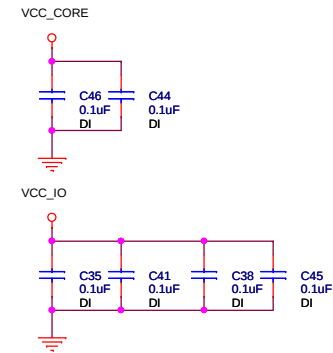
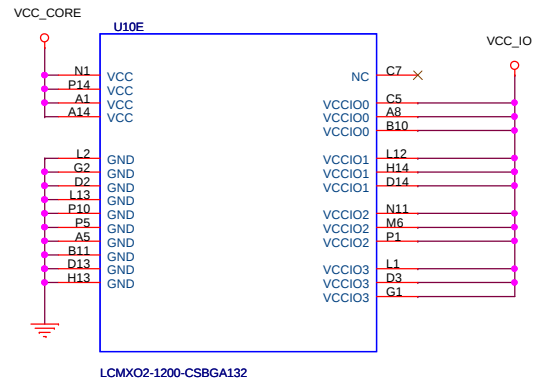
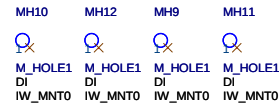
Lattice Semiconductor Applications
Email: techsupport@latticesemi.com
Phone (503) 268-8001 -or- (800) LATTICE

Title		
XO2 Bank 2-3, Cap Pads, Expansion Header, SPI		
Size	Project	Schematic Rev
B	MACHXO2 Pico Board	A
Date	Board Rev	Sheet
Friday, March 4, 2011	E	5 of 6

Board Logos



Board Mounting Holes



Lattice Semiconductor Applications
Email: techsupport@latticesemi.com
Phone (503) 268-8001 -or- (800) LATTICE

Title XO2 Power		
Size B	Project MACHXO2 Pico Board	Schematic Rev A
Date: Friday, March 4, 2011	Sheet 6 of 6	Board Rev E