Application Note

Designing PowerSage® into NAS Servers to Reduce Power Consumption

Executive Summary

Packet Digital's PowerSage® technology has been shown to substantially reduce power consumption in Network Attached Storage (NAS) servers compared to designs with conventional voltage regulators. This application note describes how to easily design Packet Digital's power management integrated circuit (PMIC) into a NAS server to reduce power consumption. Benefits of reduced power consumption are reduced temperature rise and data center operational costs through less cooling.

Figure 1: PowerSage PMIC

1 PowerSage Introduction

Packet Digital's PowerSage line of products are highly integrated power management ICs with step-down PWM controllers. Interfaces for monitoring activity, coupled with advanced On-Demand Power® algorithms, enable the regulated output voltages of the integrated switching regulators to be adaptively scaled in correlation with actual power demand. The real-time tracking of supply voltage to activity enables maximum power savings by minimizing the power spent on maintaining worst-case headroom for NAS server storage and memory power distribution. Integrating PowerSage PMICs into a NAS server saves power during both active and idle states for HDDs and memory modules. Just one dual-channel PowerSage PMIC can be used to power multiple HDDs and memory banks.

2 Reference Documents

- PSG5220 and PSG5320 Datasheets
- PSG5220 and PSG5320 Layout Guidelines
- Setting On-Demand Power Registers Application Note

3 Design Implementation

PowerSage PMICs are well suited for use in NAS Servers, specifically for providing the DDR memory bus (i.e. DDR and memory controller) voltage and the 5V supply for the HDDs with a single PMIC. Large energy spikes are seen during memory read/writes and accessing the HDD. On-Demand Power operation, integrated in the PowerSage PMIC, allows the regulated output voltage to autonomously adapt to the large spikes while lowering overall power consumption by scaling the voltage down during times of less energy need. Compared to competing solutions of providing static voltage regulation, the PowerSage PMIC will significantly reduce energy consumption.

3.1 Power Connections

PowerSage PMICs support wide input voltage ranges. The input power to the PowerSage PMIC for the memory modules and HDDs are provided by the the bulk 12V on the server power supply.

Analog circuitry and I/O in the PowerSage PMIC operate at 5V. PowerSage PMICs often have a 5V LDO, which in addition to powering the analog circuitry, can be used to power other low current fixed 5V devices.

Internal digital logic is powered at 1.8V. The PowerSage PMIC supplies this voltage through an internal linear regulator and should not be connected to an external 1.8V supply. The linear regulator output, LDO1V8, must be connected to VDD and be appropriately decoupled as described in the appropriate PowerSage PMIC datasheet.

Table 1 summarizes the power connections to the PowerSage PMIC.

Table 1: Power Connections to the PowerSage PMIC

Description	Voltage	PowerSage PMIC Lead	NAS Server Bulk Supply
Analog and I/O Input Supply Voltage	5V	V50	N/A – supplied by PowerSage PMIC
Input Voltage	6.5V to 24V	V_{IN}	12S
Digital Input Supply Voltage	1.8V	V18	N/A – supplied by PowerSage PMIC
HDDs	5V	PowerSage PMIC V_{OUT1}	N/A – supplied by PowerSage PMIC
Memory Modules	1.8V	PowerSage PMIC V_{OUT2}	N/A – supplied by PowerSage PMIC

3.2 Connections to I/O

The PowerSage PMIC autonomously scales the voltage supplied to the HDDs and memory modules based on information gathered from sensing current and activity. The activity inputs, nACT1 and nACT2, provide activity information from the HDDs (5V) and memory modules (1.8V, 1.5V, 1.35V, depending on DDR) to PowerSage. Connect the activity indicator signal to nACT with a 10k pull-up resistor to 1.8V at LDO1V8. The PowerSage PMIC will operate without the nACT signals, but the full potential for energy savings may not be fully realized, and is therefore not recommended. Do not leave nACT floating. Pull-up to LDO1V8 when not in use.

Communication to the register map is provided via the SMBUS interface through the SMBDAT and SMBCLK pins. System designers can choose to connect these directly to the Embedded Controller or through an SMBUS hub. The SMBUS pull-up resistors should be connected to the 5V LDO on the PowerSage PMIC.

3.3 Current Sense Resistor Sizing

PowerSage PMICs typically include current sensing circuitry to monitor load current in real time. The current sense resistor and applicable circuitry for each channel should be sized appropriately for the specific load that will be powered by the channel. For example, a smaller sense resistor should be used when multiple HDDs or memory modules are ran in parallel from a single channel of the PowerSage PMIC to ensure the input differential voltage of the current sense circuit remains in the 80mV working range ($10mV < V_{TRIP} < 90mV$).

4 On Demand Power Configuration

Packet Digital developed its innovative, patented On-Demand Power technology to reduce power consumption by autonomously monitoring systems using voltage scaling, distributing only the amount of power needed as demand for energy changes.

On-Demand Power technology unobtrusively senses activity within the system and correlates

to the NAS Server's HDDs and memory modules demand for energy. Once the energy demand is determined, then the PowerSage PMIC will provide dynamic voltage scaling at the power supply to provide load management.

4.1 SMBUS Serial Communication

PowerSage PMIC internal registers are programmable via SMBUS to control On-Demand Power circuitry. Activity on each domain or channel is monitored by current sense and activity inputs. Please refer to the appropriate PowerSage PMIC datasheet for SMBUS communication specifications.

4.2 Configuration Registers

A number of configuration registers must be set for the On-Demand Power circuitry to run properly in PowerSage PMICs. Voltage, threshold, and timeout registers can be set through the SMBUS interface. Packet Digital can supply the appropriate configurations for specific HDDs and memory modules.

Output voltage will vary based on system demand, managed by On-Demand Power algorithms. For more information on configuration of registers, please see the “Setting On-Demand Power Registers” application note.

5 Application Circuit

Figure 2 shows the PSG5220 5V and 1.8V application schematic. Other PowerSage PMIC application circuits will be similar.

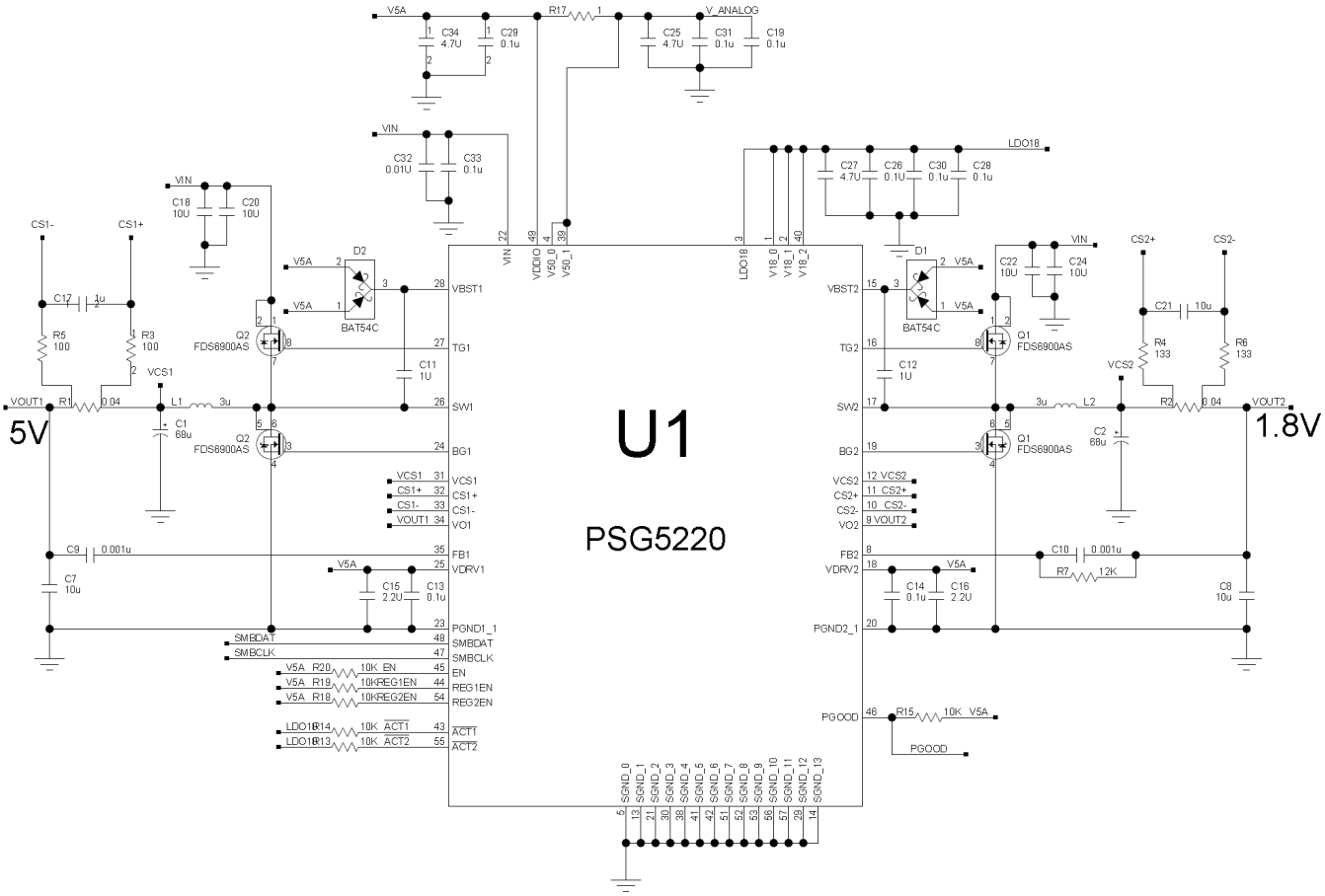

Figure 2: PSG5220 5V and 1.8V Application Circuit

6 Sample Layout

Figure 3 is a typical 4-layer printed circuit board layout for the PSG5220, but is representative of other PowerSage PMICs as well. Care should be taken to minimize the trace length of high speed switching nodes and critical nets. Please contact Packet Digital for detailed layout guidelines.

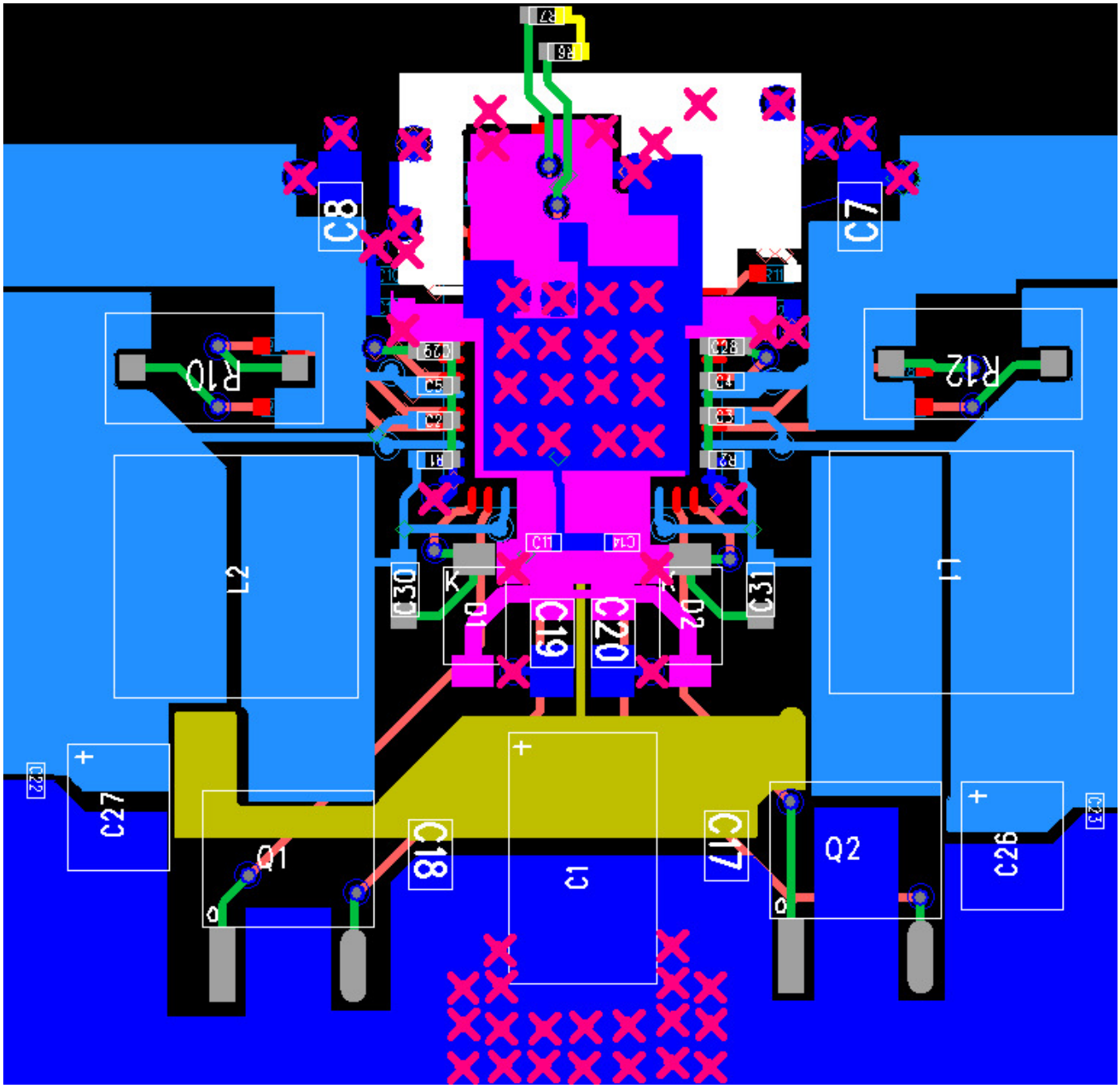

Figure 3: Sample Layout for PSG5220

7 Case Study – Integration of PSG5220 into a NAS Server

Packet Digital integrated two PSG5220 Evaluation Kits (EK) into an Iomega StorCenter Pro ix4-200r 19" rackmount server. Multiple EKs were used because of the distance between the HDDs and the memory module in this pre-designed server. The four HDDs were powered by V_{OUT1} of EK1. The memory module was powered by V_{OUT2} of EK2.

7.1 HDD PowerSage Integration

PowerSage circuitry has repeatedly been shown throughout industry to reduce power on spinning media applications. These were the steps Packet Digital used to integrate PSG5220 into the NAS server to reduce power on the HDD array:

- We used a spare 4-pin ATX power connector to provide V_{IN} (yellow wire), V5A (red wire) and ground (black wires) to the PSG5220 EK.
- V_{OUT1} of the EK was used to replace the 5V wire in the harnesses 4-pin ATX connector and then connected to the HDD array board.

These connections are shown in Figure 4.

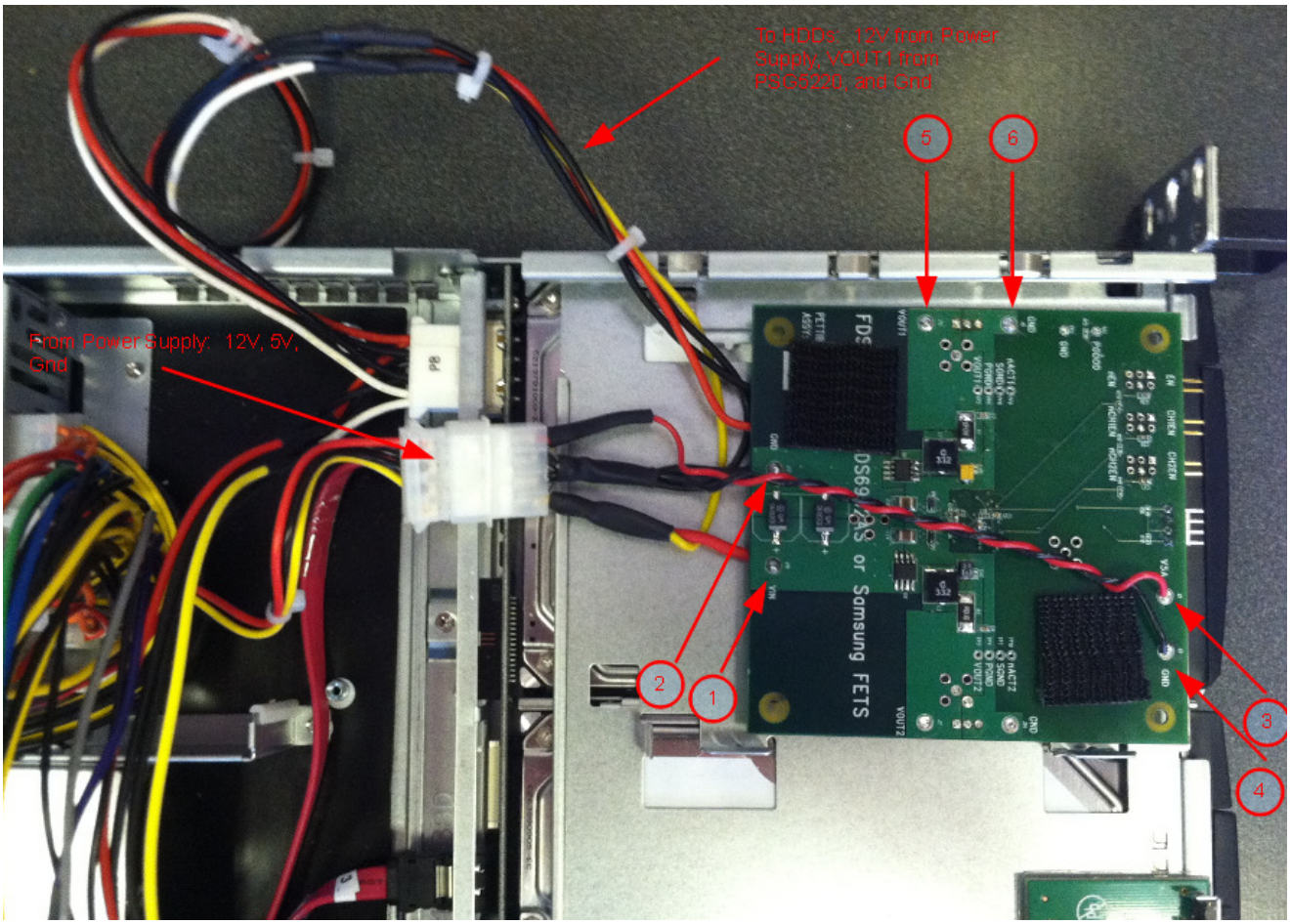

Figure 4: HDD Power Hook Up

Once the PSG5220-EK was installed, the internal registers were programmed over the SMBUS with the codes found in Table 2. Refer to the PSG5220 datasheet for the SMBUS communication specifications.

Table 2: HDD Programming Codes

Address	Data	Description
0x06	0x3C	Active Voltage, 4.4V
0x07	0x49	Idle Voltage, 4.25V
0x0B	0x41	Current Threshold, 800mA
0x0C	0x41	Current Threshold, 800mA
0x10	0x1F	Falling Slew Rate
0x12	0x50	ODP Timeout
0x13	0xC3	ODP Timeout
0x16	0x50	ODP Timeout
0x17	0xC3	ODP Timeout
0x1F	0x82	ODP Initial Slew Rate & Delay
0x03	0x09	Enable ODP

7.2 Memory Module PowerSage Integration

These were the steps Packet Digital used to integrate PSG5220 into the NAS server to reduce power on the memory module:

- A spare 4-pin ATX power connector was used to provide V_{IN} (yellow wire), V5A (red wire) and ground (black wires) to the PSG5220 EK.
- The integrated regulator's inductor, L2, was removed.
- V_{OUT2} of the EK was attached to the output capacitor side of the removed inductor's pad.
- Ground for V_{OUT2} was attached to the source of MOSFET Q29.
- It should be noted that the PSG5220 is designed for a 5V nominal output. To achieve the 1.8V necessary for memory, resistor R7 from Figure 2 must be placed in parallel with feedback capacitor C10.

These connections are shown in Figure 5.

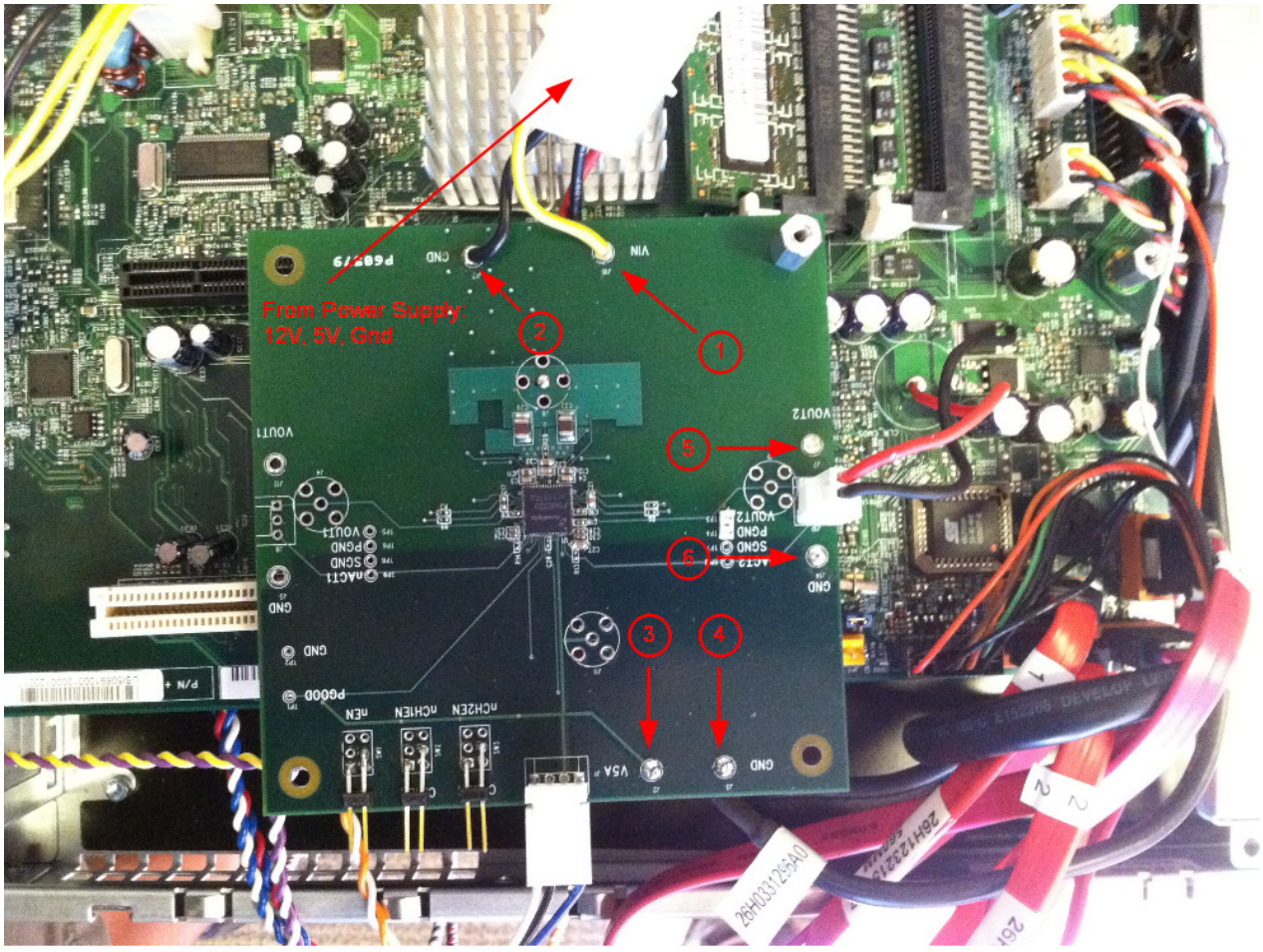

Figure 5: Memory Module Power Hook Up

Once the PSG5220-EK was installed it was programmed over the SMBUS with the codes from Table 3. Refer to the PSG5220 datasheet for SMBUS communication specifications.

Table 3: Memory Module Programming Codes

Address	Data	Description
0x25	0xB0	Active Voltage, 1.495V
0x26	0xB6	Idle Voltage, 1.484V
0x2A	0x35	Current Threshold, 900mA
0x2B	0x35	Current Threshold, 900mA
0x2F	0xFF	Falling Slew Rate
0x31	0x12	ODP Timeout
0x32	0xC3	ODP Timeout
0x35	0x50	ODP Timeout
0x36	0xC3	ODP Timeout
0x3E	0x82	ODP Initial Slew Rate & Delay
0x22	0x09	Enable ODP

8 Test Results

Packet Digital integrated PSG5220 into an Iomega StorCenter Pro ix4-200r 19” rackmount server. Baseline test results, with On-Demand Power disabled were done in idle, 90% active, and 100% active states and then repeated with On-Demand Power enabled. Table 4 displays the power savings results. Average savings were from 750mW to 1160mW!

Table 4: PSG5220 NAS Server Power Savings

Server Usage Model	Baseline Power (W)	On-Demand Power (W)	Power Savings (W)
Idle	11.60	10.86	0.75
90% Active	17.25	16.41	0.84
100% Active	18.04	16.88	1.16

9 Wrap-up

The PSG5220 is designed specifically to save power on HDDs so it is a perfect fit to reduce the power consumed by server HDDs. Additionally, the brilliance of PowerSage circuitry is its voltage scaling and power sensing capabilities which correlates very well to memory activity.

Not only does a PowerSage PMIC reduce the power consumption of the HDDs and the memory module in the NAS server, it also extends the life of the server by reducing the ambient temperature which has the added benefit of reducing the air conditioning costs over the life of the server in the data center.

10 Contact info

Packet Digital's world-wide engineering support team will assist you in integrating a PowerSage PMIC into your design. Please contact Packet Digital with any questions or for the latest reference design and layout guidelines.

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