Using the PE42920 in Digital Applications

Application Note 53

Summary

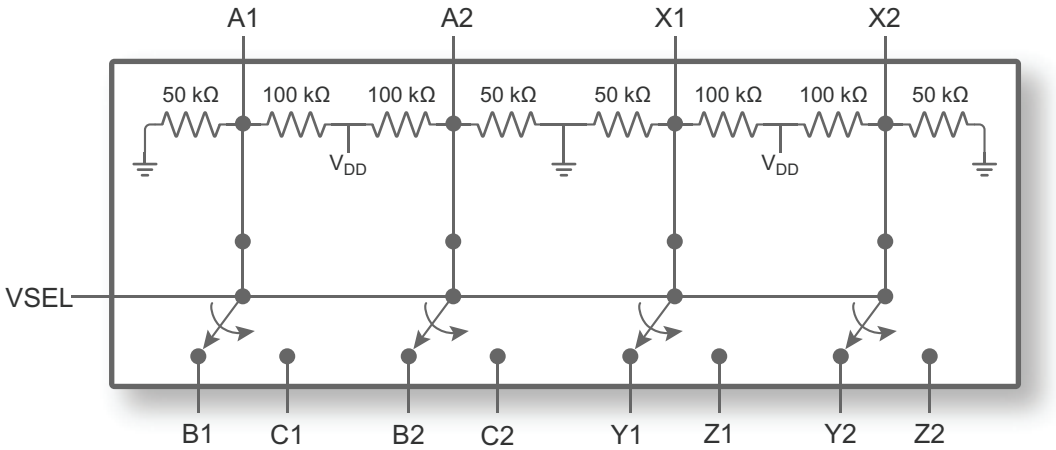
The PE42920 can be used in a variety of high-speed data applications, including 10G Ethernet, PCI Express Gen 3, USB 3.0, SAS/SATA 6G, DisplayPort, 3G SDI and Fiber Channel 8.5G. This application note provides the specifications and performance of the PE42920 for these applications.

Introduction

The PE42920 is a high bandwidth, low power, dual differential single pole double throw (DDSPDT) passive switch. The DDSPDT is controlled using a single select pin operating from a single 3.3V power supply. The switch supports up to 10 Gbps data rate, making it ideal for many high-speed data applications. It provides 6 GHz bandwidth data paths that can be used for routing and switching of very high-speed NRZ data. The PE42920 consumes less than 2 mW of power during normal operation.

The PE42920 is offered in a standard green, RoHS-compliant 16-lead 3 × 3 mm QFN package. The device pinout is architected to enable optimized PCB routing while providing maximum crosstalk isolation. Crosstalk isolation is critical for successful data transmission at multi-gigabit speeds.

Figure 1 • *PE42920 Functional Diagram*



Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in Table 1 may cause permanent damage. Operation should be restricted to the limits in Table 2. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Table 1 • *Absolute Maximum Ratings*

Parameter	Min	Typ	Max	Unit
Supply voltage, V_{DD}	–0.5		4	V
DC on current data pins, I_{SW}			4	mA
Storage temperature, T_{STORE}	–65		+150	°C
ESD voltage HBM(*), V_{ESD}			2000	V

Note: * Human body model (MIL_STD 883, Method 3015).

Recommended Operating Conditions

Table 2 lists the recommending operating condition for the PE42920. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 • *Operating Ranges*

Parameter	Min	Typ	Max	Unit
Supply voltage, V_{DD}	2.97	3.3	3.63	V
DC current on data pins, V_{SW}			3	mA
Operating case temperature, T_{CASE}	–40		+85	°C

Electrical Specifications and Performance

Table 3 and Table 4 provides the PE42920 key electrical specifications and performance. Unless noted otherwise, typical test conditions in this application note are +25 °C case temperature, V_{DD} = 3.3V, 800 mV differential input data swing (V_{IH_DATA} = 200 mV), nominal (800 mV_{PPD}) output swing, PRBS 2^7—1 test pattern with R_{LOAD} = 50Ω, short traces and/or cables, AC coupled I/O. Minimum and maximum performance are tested over temperature at –40 °C to +85 °C, and V_{DD} = 2.97–3.63V.

Table 3 • *Power Consumption Specifications*

Parameter	Min	Typ	Max	Unit
Quiescent power supply current, I_{DD}		100	500	µA
DC power consumption, P_{TOTAL}		0.33	1.8	mW

Table 4 • *Input/Output (I/O) Performance*

Parameter	Min	Typ	Max	Unit
Input high voltage on VSEL pin, V_{IH} (*)	0.7 × V_{DD}		V_{DD}	V
Input low voltage on VSEL pin, V_{IL} (*)	0		0.3 × V_{DD}	V
Differential peak to peak input data swing (AC coupled), V_{PPD}			2.8	V
Input high voltage on data pins, V_{PEAK}, AC coupled, V_{IH_DATA}			700	mV
Common-mode voltage on data pins if DC coupled (V_{DD}/3), V_{CM_DATA}	0.99	1.1	1.21	V
Switching time, t_{SW} (*)		0.3	0.5	µs
Bit-to-skew within the same differential pair, $t_{SKEW,PN}$		8	15	ps
Channel-channel skew, $t_{SKEW,CH}$		12	25	ps
3 dB bandwidth, BW	5.6	6		GHz
Crosstalk at 0–6 GHz (A to X), X_{TALK}		–30	–25	dB
OFF isolation at 0–6 GHz (A/X to C/Z with B/Y enabled), OIRR	24	26		dB
Insertion loss @ DC, SDD21		0.7	1.25	dB
Differential return loss at 50 MHz–1.25 GHz, SDD11	12.5	14		dB
Differential return loss at 1.25–2.5 GHz, SDD11	8	9		dB
Differential return loss at 2.5–4 GHz, SDD11	5	8		dB

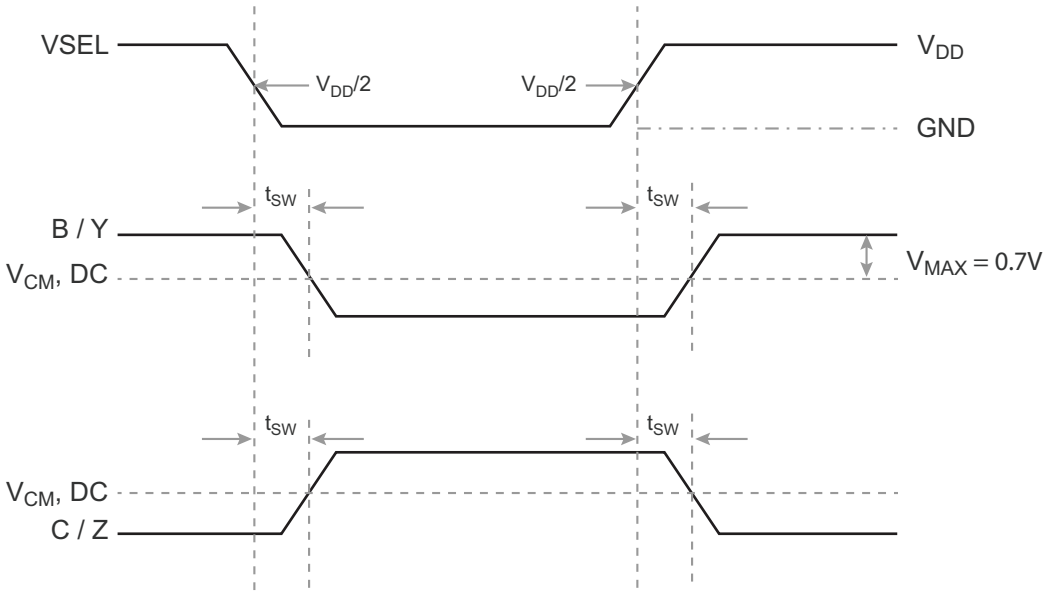
Table 4 • *Input/Output (I/O) Performance (Cont.)*

Parameter	Min	Typ	Max	Unit
Common mode return loss at 50 MHz–2.5 GHz, SCM11	12	14		dB
Common mode return loss at 2.5–4 GHz, SCM11	10.5	13		dB
ON resistance of the switch, RON		8.5	15.5	Ω
ON resistance match between same pair, Δ_{RON}		0.3	0.5	Ω
ON resistance match between channels, $\Delta_{RON,CH}$		0.3	0.8	Ω
Note: * Control pin specifications.				

Enable and Disable Timing Diagram

Figure 2 shows the response of the high signal path when the VSEL pin is switched. When VSEL is set low B/Y will be disabled after time t_{SW} (as specified in Table 4) and C/Z will be enabled after time t_{SW}. When VSEL is set high C/Z will be disabled after time t_{SW} and B/Y will be enabled after time t_{SW}.

Figure 2 • *Enable and Disable Timing Diagram*



Typical Performance Data

Figure 3–Figure 26 show the typical performance data @ +25 °C case temperature, V_{DD} = 3.3V, unless otherwise specified.

Figure 3 • ***Eye Diagram at 5 Gbps, 2 dB of De-emphasis***

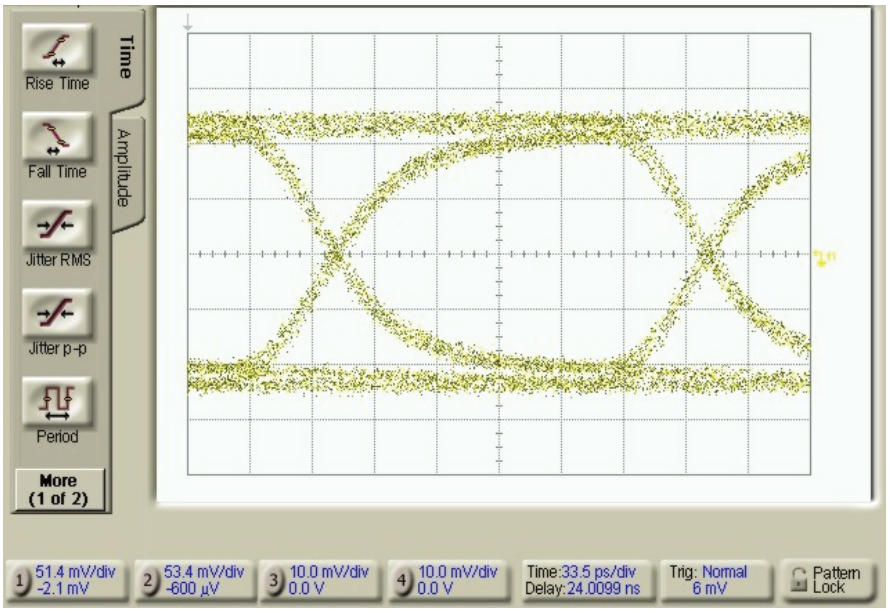


Figure 4 • ***Eye Diagram at 8 Gbps, 2 dB of De-emphasis***

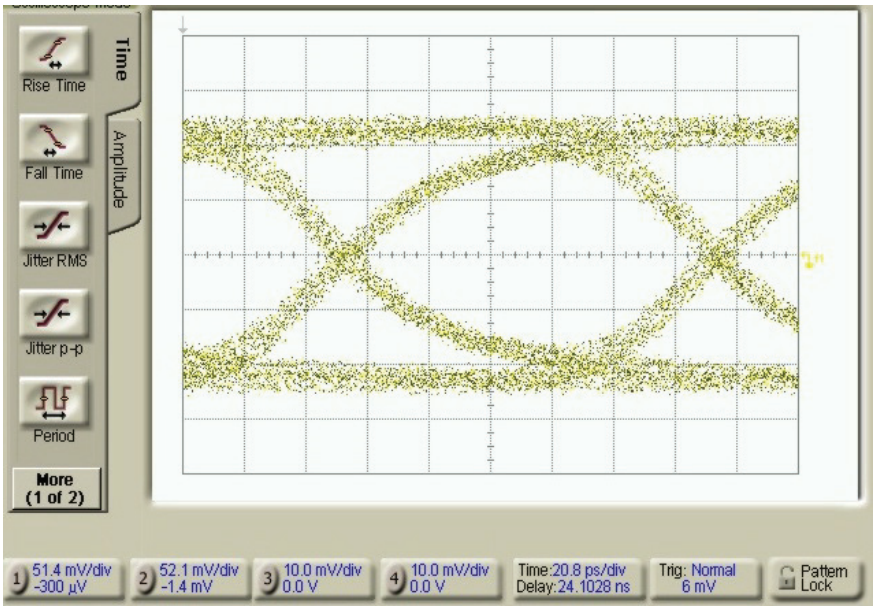


Figure 5 • *Eye Diagram at 10 Gbps, 2 dB of De-emphasis*

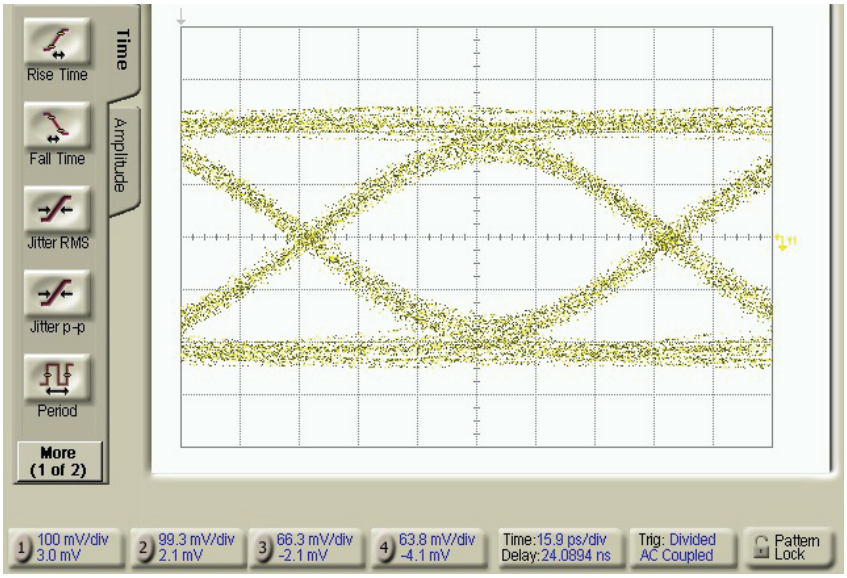


Figure 6 • *Eye Diagram at 12 Gbps, 2 dB of De-emphasis*

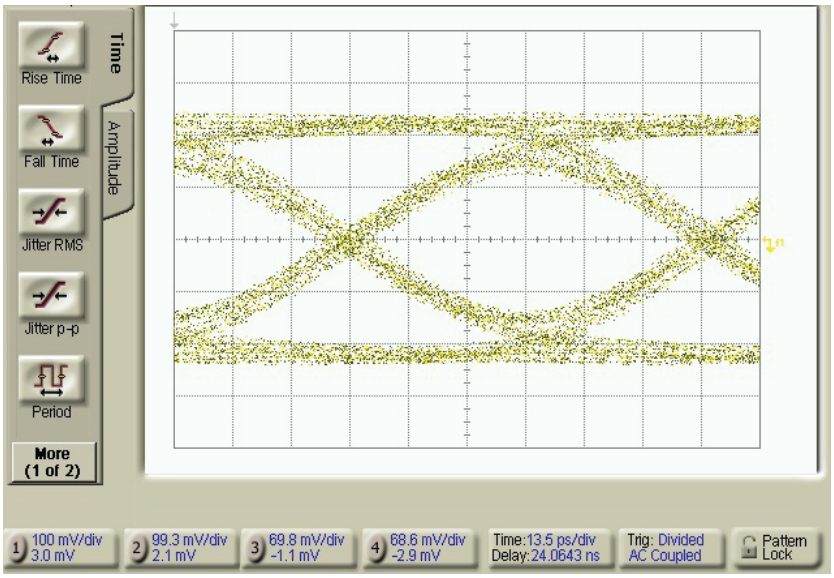


Figure 7 • *Insertion Loss vs Temperature (A to B)*

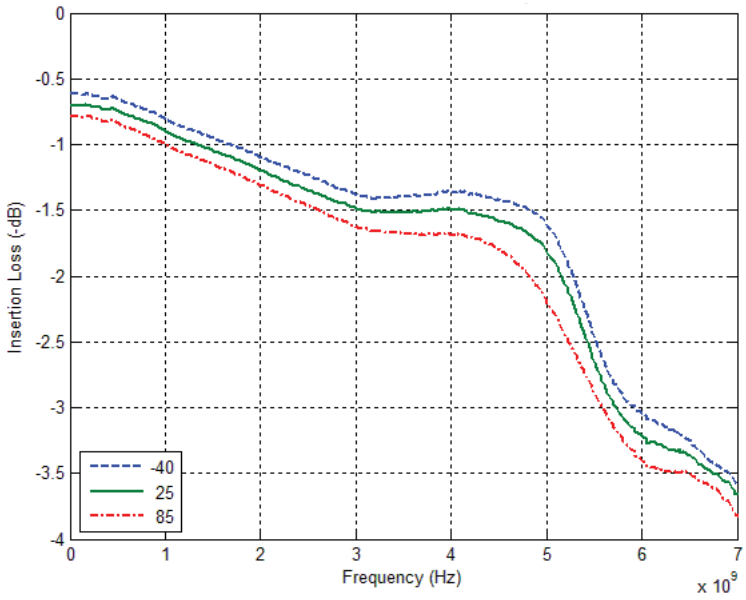


Figure 8 • *Insertion Loss vs V_{DD} (A to B)*

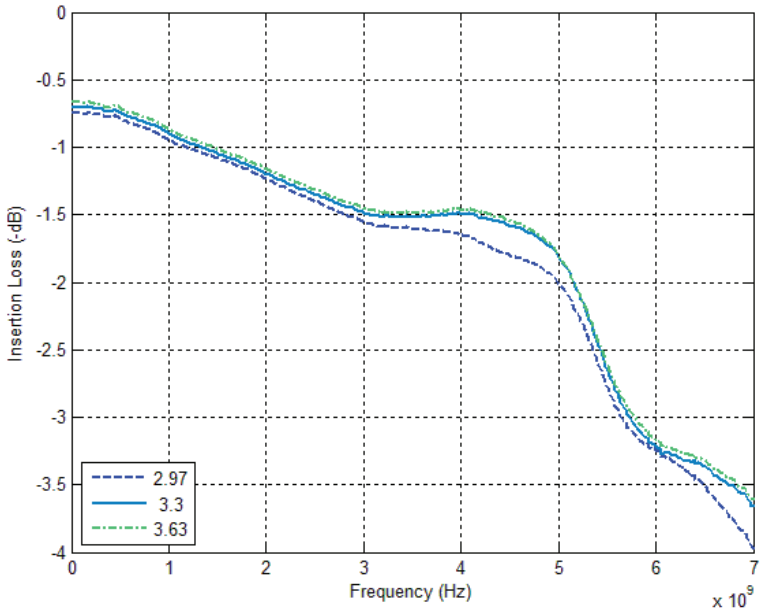


Figure 9 • *Return Loss vs Temperature (A to B)*

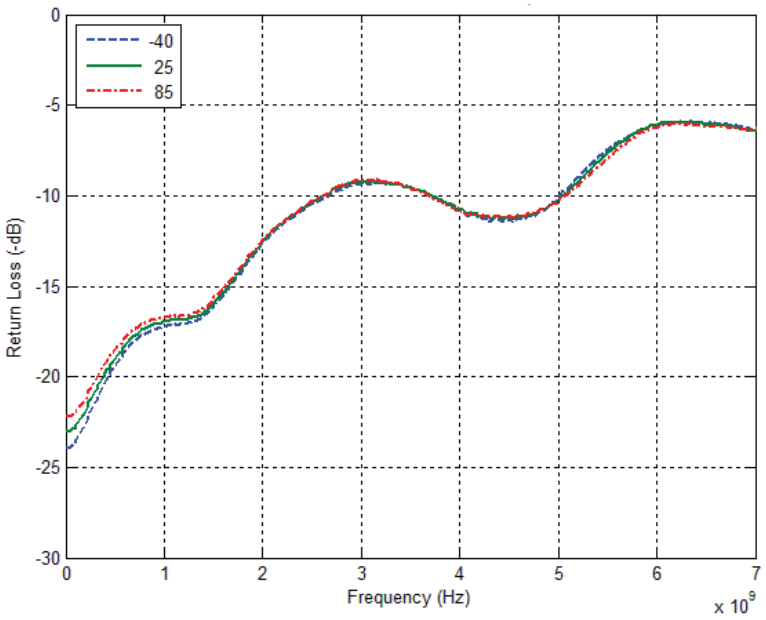


Figure 10 • *Return Loss vs V_{DD} (A to B)*

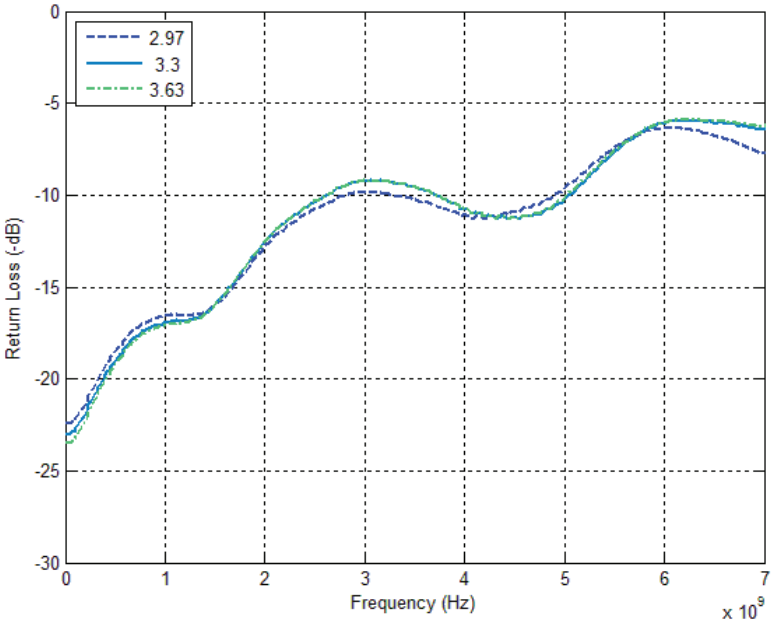


Figure 11 • *Insertion Loss vs Temperature (A to C)*

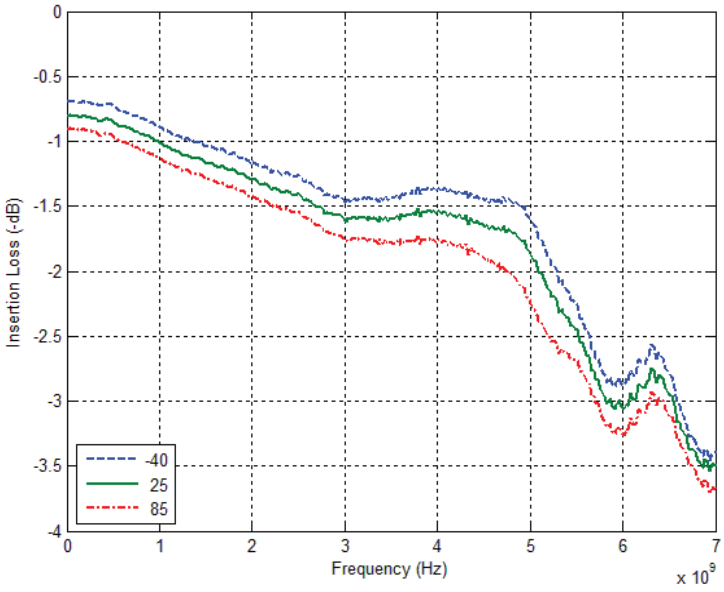


Figure 12 • *Insertion Loss vs V_{DD} (A to C)*

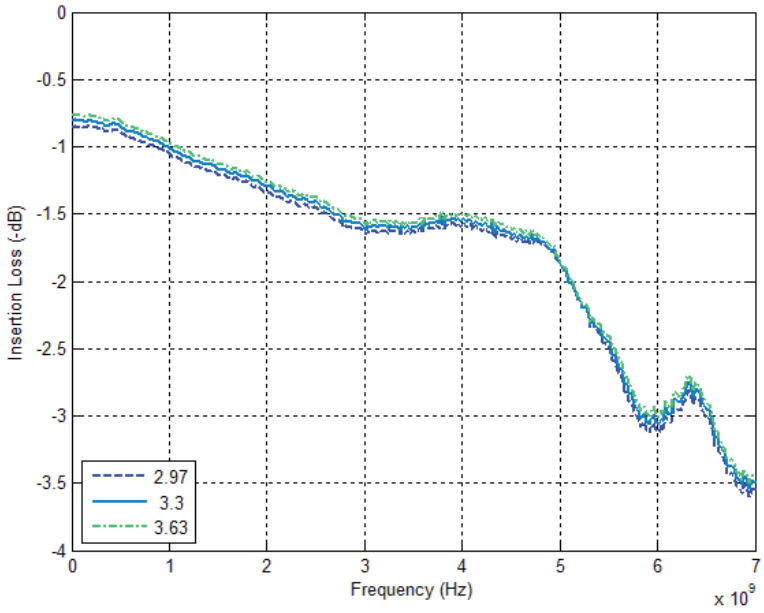


Figure 13 • *Return Loss vs Temperature (A to C)*

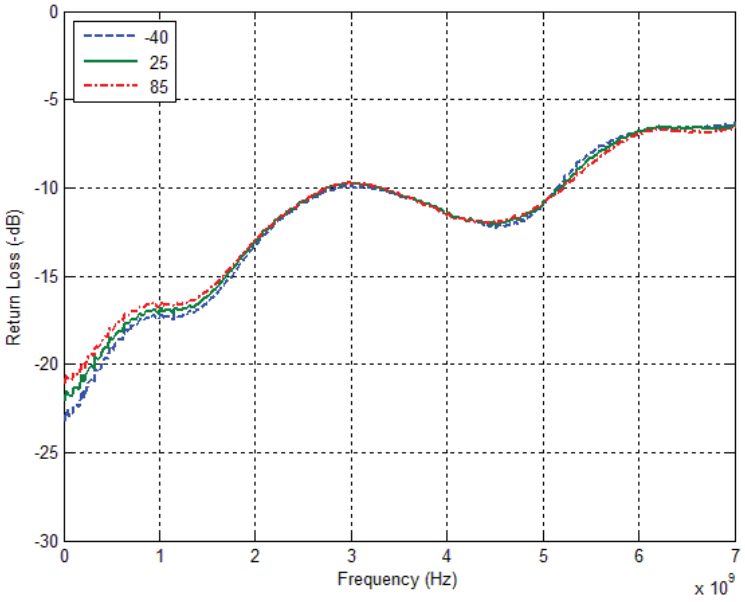


Figure 14 • *Return Loss vs V_{DD} (A to C)*

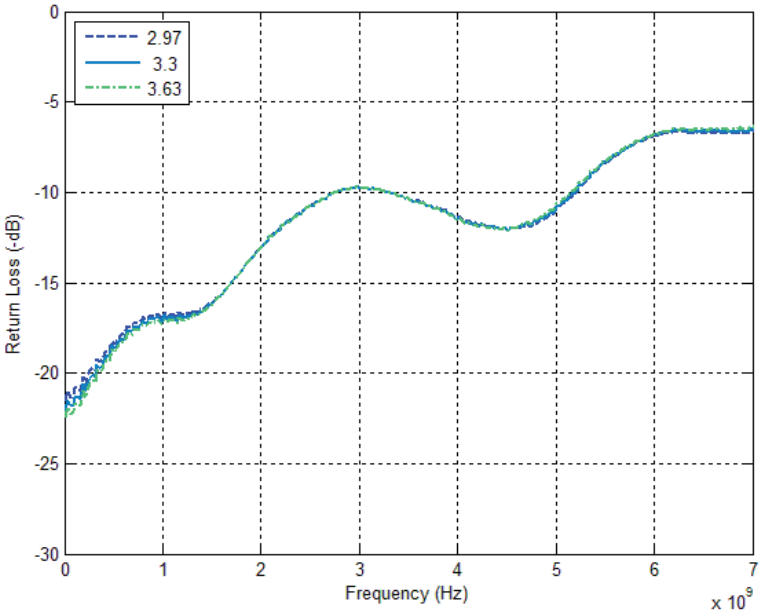


Figure 15 • *Insertion Loss vs Temperature (X to Y)*

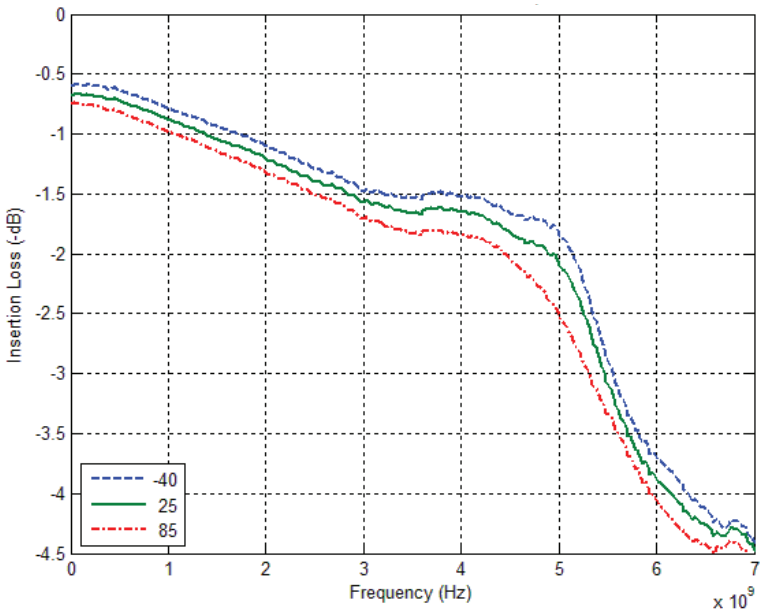


Figure 16 • *Insertion Loss vs V_{DD} (X to Y)*

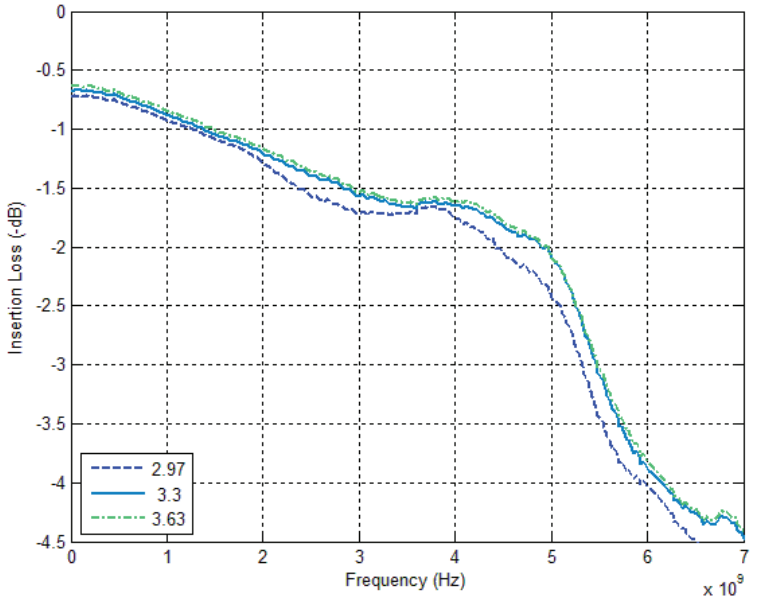


Figure 17 • *Return Loss vs Temperature (X to Y)*

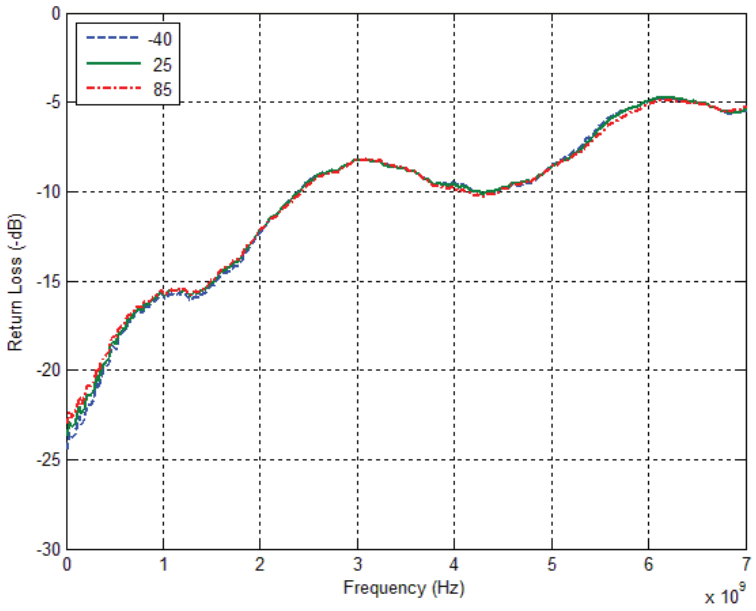


Figure 18 • *Return Loss vs V_{DD} (X to Y)*

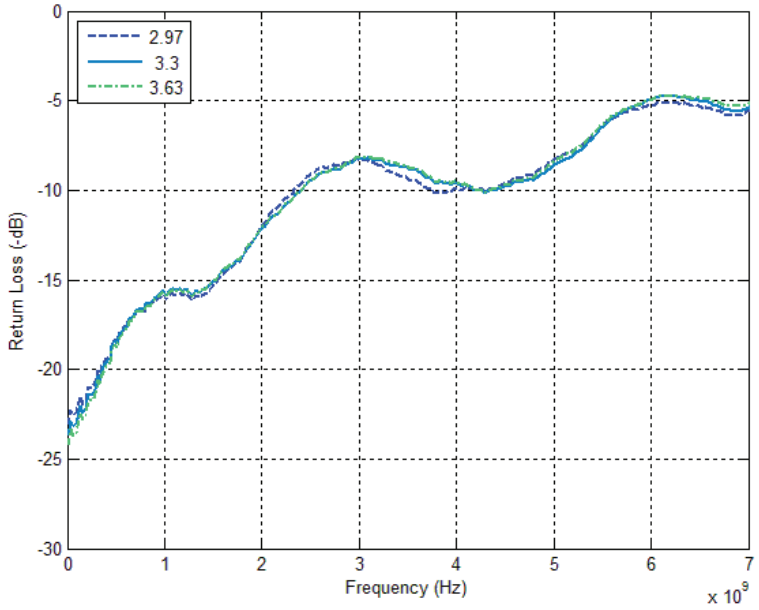


Figure 19 • *Insertion Loss vs Temperature (X to Z)*

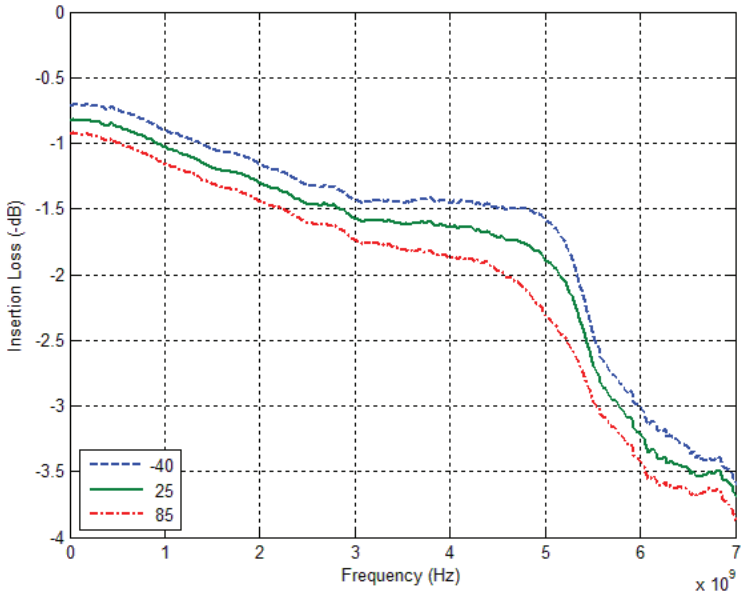


Figure 20 • *Insertion Loss vs V_{DD} (X to Z)*

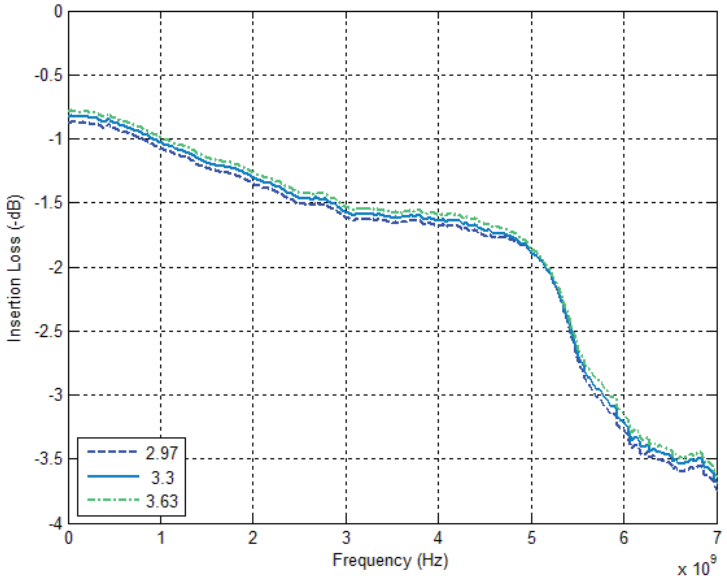


Figure 21 • *Return Loss vs Temperature (X to Z)*

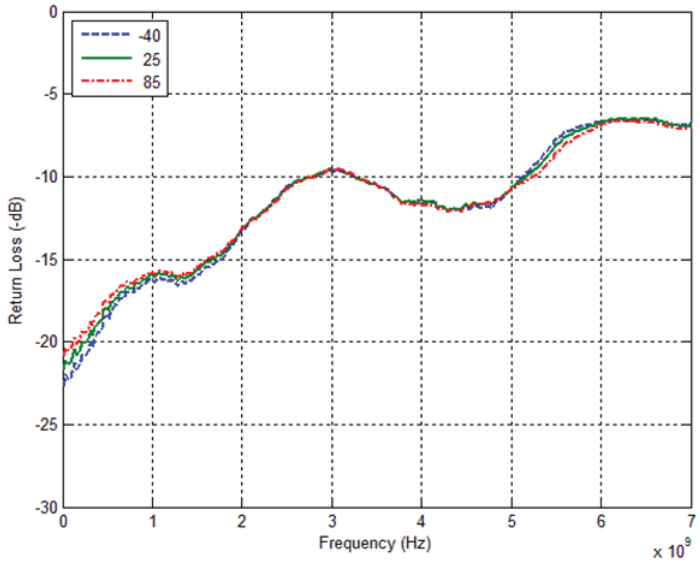


Figure 22 • *Return Loss vs V_{DD} (X to Z)*

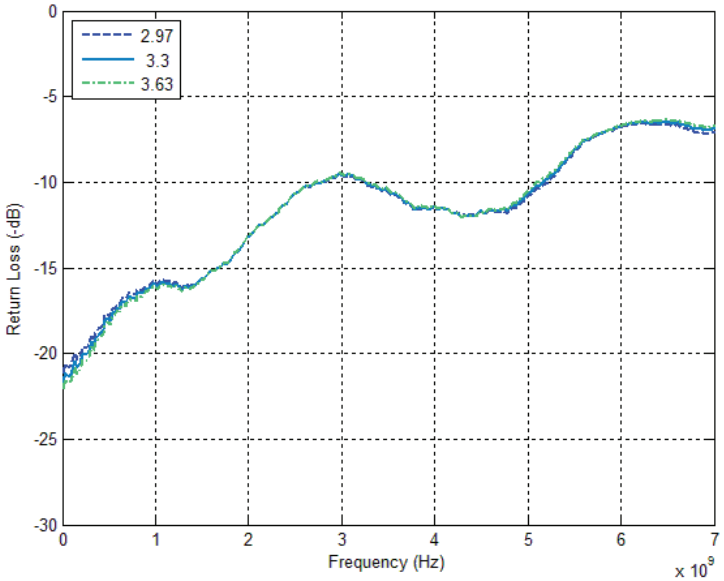


Figure 23 • *Opposite Channel Isolation vs Temperature (A to X)*

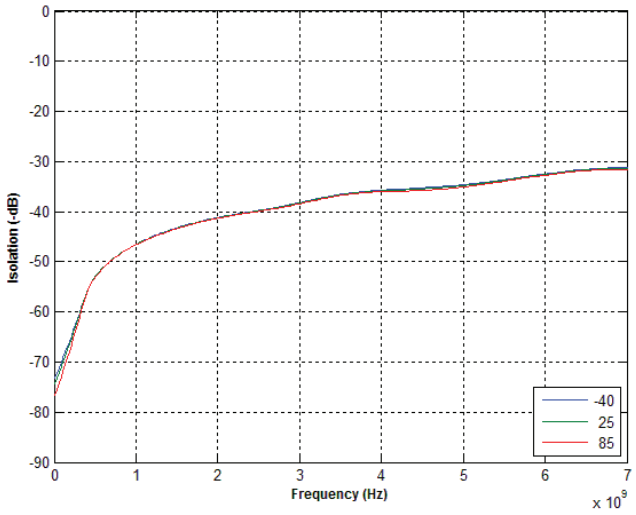


Figure 24 • *Opposite Channel Isolation vs V_{DD} (A to X)*

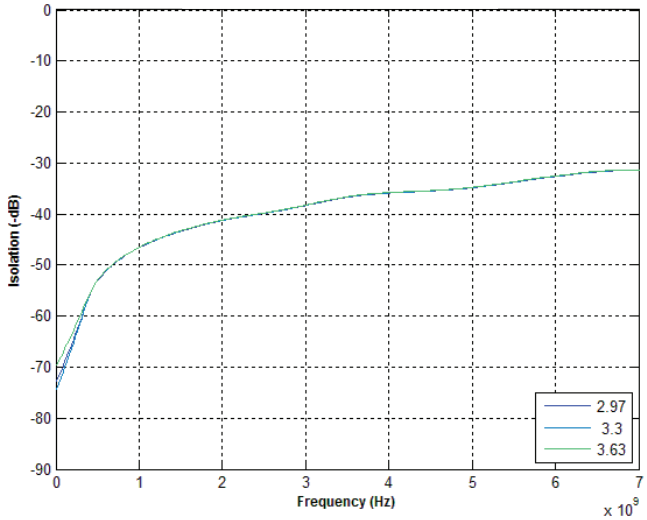


Figure 25 • *Same Channel Isolation vs Temperature (A to C/B and X to Z/Y)*

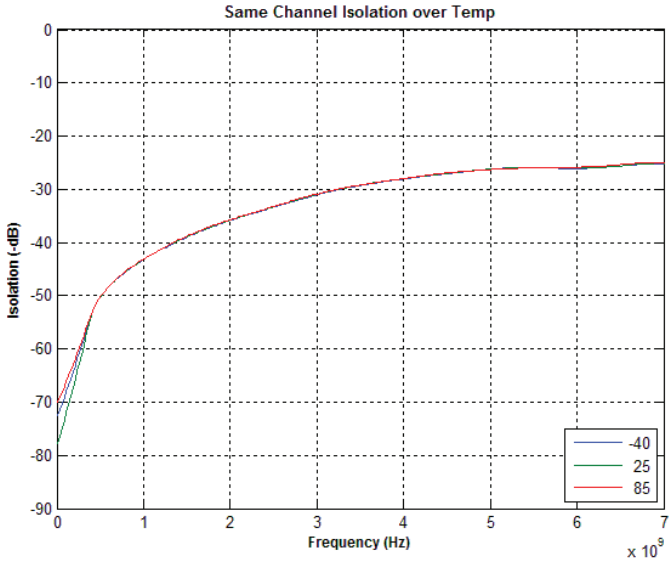
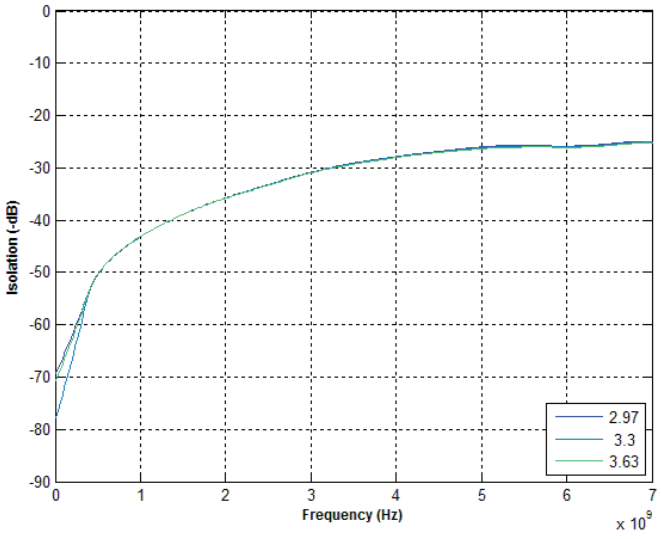


Figure 26 • *Same Channel Isolation vs V_{DD} (A to C/B and X to Z/Y)*



Conclusion

The PE42920 offers excellent features to support high-speed data applications besides RF differential switching. This application note provides the specifications and performance of the PE42920 when using it in digital applications.

The features of the PE42920 include:

- DDSPDT passive switch
- 10 Gbps data rate support
- Low power consumption of less than 2 mW during normal operation
- 6 GHz bandwidth data paths
- Single 3.3V power supply eliminates the need for additional regulation
- Small package size of 16-lead 3 × 3 mm QFN package
- Optimized pinout for PCB routing and provides maximum crosstalk isolation

Sales Contact

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