F-55471 & F-55472-STEP Series Graphic Displays

Optrex America, Inc.
46723 Five Mile Road
Plymouth, MI 48170 USA

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REVISION HISTORY

REV	DATE	PAGES	COMMENT
A	4/9/2010	1-27	Initial Release

1.0 REFERENCES

(a) Novatek NT7534 132x65 Ram-Map STN LCD Controller Driver Specification Rev 1.0

(b) Optrex F-55472 Products List

(c) Optrex F-55471 Products List

2.0 DESCRIPTION

2.1. This application note provides guidance for interfacing, programming, and using F-55471-series and F-55472-series displays. This document, along with the LCD module specification, the module drawing and LCD controller-driver technical manual, reference (a) provides the application information needed to design the display into electronic products. The document IS NOT INTENDED to be the sole source of guidance for using the display.

2.2. The LCD module drawing provides size and information for the connector(s) built in the product. The drawing does not provide the mating connector for flexible printed circuits (FPC) since there are many potential sources available.

2.3. The LCD Module Technical Specification provides electrical and optical performance specifications, cosmetic specifications, and qualification information. The controller-drivers used in the display can be interfaced in many different configurations and logic voltages. It is not possible to build and test every combination; therefore, the specification lists a configuration verified by Optrex. This document provides guidance for using various voltage supplies.

2.4. The F-55472-series displays include the following components:

Monochrome liquid crystal display panel. The displays have various color options, which vary by displaying the data image or the inverse data image. Please see FIGURE 1 for examples of each.

- Novatek NT7534 LCD Controller / Driver. Reference (a) describes controller-driver use. Optrex highly recommends downloading and studying before designing hardware and software.
- RAM to store the digital representation of the image at one bit per pixel color depth.
- DC-to-DC Boost Circuit to generate contrast voltage (feature not recommended on F-55471 displays).
- Liquid crystal driving circuitry with bias voltage generator and contrast control (via software). This feature not recommended for F-55471 displays.
- Backlight / Carrier.

2.5. FIGURE 1 shows the various colors available for the displays. The “normal data” images depict the color of the native design. The inverse data images provide appearance when the NORMAL / REVERSE DISPLAY command inverts the image by software command.

For those planning to use one design with various displays, the LCD drive voltages vary between color modes, which may affect software and hardware slightly.

2.6. The F-55471 displays increase resolution by using two controller-drivers configured for MASTER - SLAVE operation with each driving one-half of the LCD screen.

FIGURE 1 -- DISPLAY COLOR AND DATA MODES

3.0 THEORY OF OPERATION

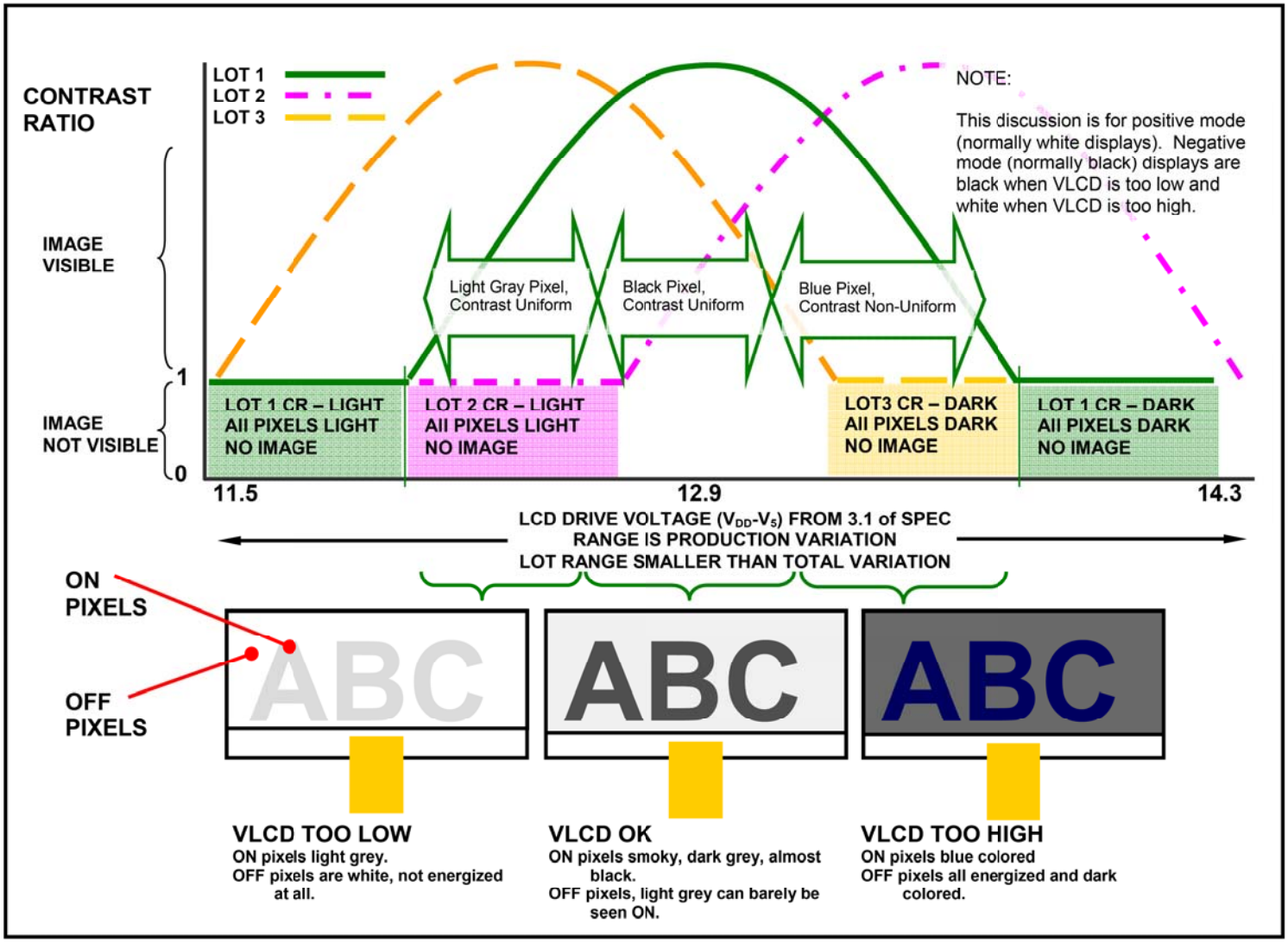
3.1. A microprocessor writes to the LCD controller, configuring it for operation and sending image data. The controller reads the RAM and automatically generates voltage waveforms to cause the liquid crystal pixels to change state. There is one data bit in RAM for each pixel location. Configure both controllers in F-55471 independently to show their portion of the image.

3.2. The liquid crystals require a complex, time-changing, high voltage waveform whose magnitude is larger than V_{DD}. This LCD drive voltage may be either internally or externally generated dependent upon the boost capability of the IC and the supplied logic voltage.

3.3. The LCD drive voltage is resistance divided to form six discrete voltages applied to the electrical traces on the glass. The difference between the voltage levels corresponds to the display bias ratio. The ON pixel voltages are V_{SS} and V_0. The OFF pixel voltages are V_1 through V_4.

3.4. Display contrast, the difference in luminance from the ON pixel state to the OFF pixel state, is controlled by varying the magnitude of the LCD drive voltage. Changing the contrast voltage causes all voltages V_0 to V_4 to change. Excess drive causes the OFF voltage levels to exceed the liquid crystal ON voltage level and change state; contrast is reduced. Excessive drive voltage also causes crosstalk as voltage bleeds from ON pixels to OFF pixels. No image is seen when insufficient voltage prevents the liquid crystals from changing state. FIGURE 2 shows the voltage to contrast ratio relationship and lot-to-lot variation. The designer must account for this variation.

FIGURE 2 -- DISPLAY CONTRAST



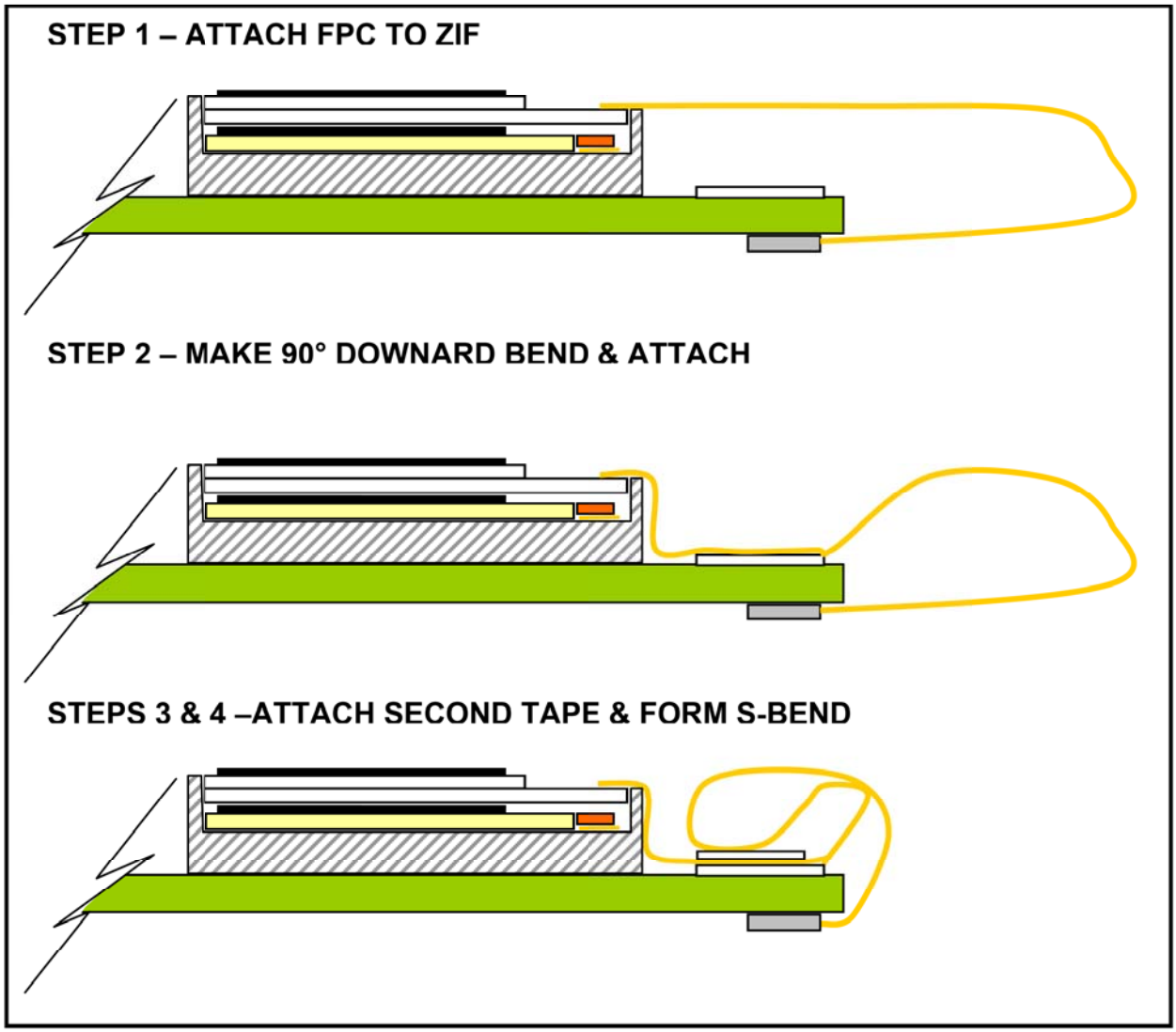
4.0 MECHANICAL CONSIDERATIONS

4.1. The display may be attached via screws or double sided adhesive. The frame is made of polycarbonate.

4.2. The flexible printed circuit (FPC) must not tightly bend and permanently deform the copper traces (form a crease). During bending, the inner sides of the copper traces are compressed while the outer sided are placed in tension. This can fracture traces and electrically open the circuit. The minimum bend radius should be 10 times the thickness of the FPC to prevent permanent deformation. The drawing dimensions the FPC as 0.3 mm thick at the stiffener. This is not the thickness where bending occurs. The FPC is 0.120 mm thick in the bend area. The minimum bend radius is 1.2 mm for a 90-degree bend. A 180° bend requires a larger radius to prevent creasing. Form small radius bends, greater than 90°, one time only. Do not un-bend.

4.3. FIGURE 3 describes a method to bend the FPC and shorten its length. The plastic frame extends 1.2 mm beyond the edge of the glass, so the FPC minimum bend radius allows a bend touching the frame.

FIGURE 3 -- FPC BENDS TO SHORTEN LENGTH.



5.0 ELECTRICAL

5.1. INTERFACE CONNECTION & VOLTAGES

5.1.1. The F-55472 displays interface via a 30-conductor FPC. A major design consideration is the contact location in the connector. The contacts may be top or bottom. The FPC contacts are on the bottom side. The designer must take FPC bending and connector location into account and choose the correct contact location when selecting connectors. Sources for compatible connectors are:

Kyocera Elco 08-6210-030-340-800 – 30 pin, zero insertion force (ZIF), right angle, bottom contact, surface mount, 0.5 mm pitch FPC, 0.30 mm thick, with front slide lock.

Molex 54132-3097 – 30 pin, zero insertion force (ZIF), right angle, bottom contact, surface mount, 0.5 mm pitch FPC, 0.30 mm thick, with front slide lock.

Omron XF2M-3015-1A – 30 pin, zero insertion force (ZIF), right angle, top & bottom contact, surface mount, 0.5 mm pitch FPC, 0.30 mm thick, with rear rotary lock.

The F-55471 interfaces via two 36-conductor FPCs. The FPC contacts are on the bottom side. Sources of compatible connectors are:

Kyocera Elco 08-6210-036-340-800 – 36 pin, zero insertion force (ZIF), right angle, bottom contact, surface mount, 0.5 mm pitch FPC, 0.30 mm thick, with front slide lock.

Molex 54132-3662 – 36 pin, zero insertion force (ZIF), right angle, bottom contact, surface mount, 0.5 mm pitch FPC, 0.30 mm thick, with front slide lock.

Omron XF2M-3615-1A – 36 pin, zero insertion force (ZIF), right angle, top & bottom contact, surface mount, 0.5 mm pitch FPC, 0.30 mm thick, with rear rotary lock.

These part numbers are presented for information only. Optrex has not tested the performance and reliability of these connectors and makes no warranty to their fitness for use. Please note that any connector matching the FPC pitch characteristics and mating tolerances may be used.

5.1.2. SPI Interface

The displays use Novatek NT7534 controller/drivers which may be configured for 8-bit parallel or 8-bit serial (SPI) communication. Selection of parallel / serial data is controlled by the P/S signal. Pull the pin high or low; do not float. Pull the pin HIGH for parallel data input or LOW for serial data. Floating the pin is known to cause timing issues.

SIGNAL	F-55471 PINS	F-55472 PINS	STATUS
P/S	34	29	Pull LOW for SPI Pull HIGH for 68- / 80s-Series
(D0 to D5)	11 to 16	7 to 11	no connect
Serial clock (SCL / D6)	12	17	
Serial data (SI / D7)	13	18	

Using SPI prevents reading the display status and RAM. It is advantageous to use the parallel interface during development in order to read the controller status and RAM. Switch to SPI after confirming EMI / EMC and ESD compatibility.

5.1.3. Voltage Regulator Gain Setting Resistors

The NT7534 has an internal voltage regulator op-amp configured as an inverting, differential amplifier as shown in FIGURE 5. Feedback resistors control amplifier gain. These gain control resistors can be selected either internally or externally. Pin 30 on the F-55472

controls selection of the internal resistors / external resistors. Pull the pin high to use the internal resistor and set the gain via software command.

If using the external resistors, pull Pin 30 Low. Connect resistors to the VR and V_0 pins to set gain as shown in FIGURE 5. The resistors must meet 1.5 MΩ ≤ R_A + R_B. If lower value resistors are used, current consumption increases.

$$GAIN = 1 + \frac{R_B}{R_A}$$

5.1.4. F-55471 Master-Slave Operation

The F-55471 operates with the master providing control signals to the slave. The following connections apply.

Pins (2) FR, (3) CL, (4) DOF – The MASTER outputs clock and frame signals to the SLAVE for synchronization purposes. These pins should be connected together from the MASTER to SLAVE using the shortest possible path length to minimize capacitance that can distort the timing waveforms. The DOF pin allows the MASTER to control the SLAVE output driver pins ON and OFF.

Do not connect the boosting capacitor pins (22 to 26). An external power supply is used to supply V_0 to V_4 for both the master and slave.

Pin (36) IRS – The IRS pin controls the use of internal resistor values used for the voltage regulator op-amp. This converter is not used since an external power supply will be used to create the LCD drive voltages. Pin 36 (IRS) should be set low for the MASTER. The IRS pin should not be connected for the SLAVE. The SLAVE pin is pulled to V_{DD} on the glass.

The NT7534 is selected when CS1 is low and CS2 is high. Please note the MASTER and SLAVE must not be selected simultaneously when writing data or commands.

5.2. LOGIC AND LIQUID CRYSTAL POWER SUPPLIES

5.2.1. The display specification lists the logic voltage at which Optrex confirmed operation, but the IC may operate at other logic voltages listed in reference (a). When other logic voltages are used, the designer must consider the amount of DC / DC boost available to set V_0 appropriately to generate the V_0-V_{ss} voltage difference to run the liquid crystals. This voltage is specified in Section 3.1 of the LCD specification. FIGURE 4 provides an example of the LCD driving voltage requirement.

Contrast voltage may be controlled via several methods depending upon the power supply setup. Power supply setup is discussed in sections 5.2.2 through 5.2.7.

Section 3.1 of the LCD specification also provides the production variation for VLCD. This means the system design must provide the range of drive voltages in order to obtain proper operation. If the V_0-V_{SS} voltage is fixed, say at 12.9 V, a display that requires 13.3 V to operate will not show an image (see FIGURE 2). By ensuring the system can provide the maximum voltage at low temperature and the minimum voltage at high temperature, production variation is accommodated. Please design the system to provide variable LCD drive voltage.

Liquid crystals exhibit temperature dependence. As temperature increases, the viscosity of the liquid crystals decreases and less voltage is required to cause the liquid crystal to change state. The drive voltage must reduce or else contrast suffers. As temperatures decrease, the voltage must increase. The NT7534 has -0.05 % temperature compensation of V_0. The temperature compensation does not perfectly match the liquid crystal temperature characteristics so the electronic volume should vary to control contrast. See Section 6.6 for recommended settings.

If an external power supply is used, consider adding temperature compensation to maintain best contrast performance.

FIGURE 4 -- LCD DRIVING VOLTAGE VS TEMP

3.Optical Specifications

3.1.LCD Driving Voltage

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Recommended	V_{DD}-V_5	Ta= -20°C	-	-	14.3	V
LCD Driving Voltage		Ta=25°C	12.0	12.9	13.8	V
Note 1		Ta=70°C	11.5	-	-	V

Note 1 : Voltage (Applied actual waveform to LCD Module) for the best contrast. The range of minimum and maximum shows tolerance of the operating voltage. The specified contrast ratio and response time are not guaranteed over the entire range.

5.2.2. FIGURE 5 shows the NT7534 LCD drive voltage generating circuits. The IC features include:

- A DC-to-DC boost circuit for generating a large voltage available on V_{OUT}. V_{OUT} is supplied to the voltage regulator op-amp as one rail voltage. V_{SS} is the other rail voltage. If desired, the designer may supply V_{OUT} externally. An external V_{OUT} must meet $V_{OUT} - V_{SS} > (MAX [V_{OUT} - V_0] + 0.1 V)$.
- A voltage regulator. This circuit can adjust the magnitude of the LCD drive voltage, V_0-V_{SS}, to control contrast by setting an ELECTRONIC VOLUME register value via software. The designer also has the option to provide this voltage externally to the V_0 pin.
- A voltage follower. This circuit generates the drive voltages (V_0 to V_4, & V_{SS}) needed to run the liquid crystals. If desired, the designer may supply the six voltages externally as shown in FIGURE 8.

There are eight possible combinations of these features. In practice, there are three practical combinations based upon the V_{DD}, boost capability, and the required liquid crystal drive voltage.

POWER CONTROL OPTION 1 – DC-to-DC Boost ON, Voltage Regulator ON, Voltage Follower ON. This configuration minimizes external components.

POWER CONTROL OPTION 2 – DC-to-DC Boost OFF, Voltage Regulator ON, Voltage Follower ON. Consider this option if image quality requires improvement.

POWER CONTROL OPTION 3 – DC-to-DC Boost OFF, Voltage Regulator OFF, Voltage Follower OFF. This option is recommended for F-55471 displays. This option may also be used with F-55472 displays for best possible image performance.

See FIGURE 7 for schematic depictions of these options.

5.2.3. The F-55472 has sufficient boost capability to use the internal DC-to-DC booster, voltage regulator and voltage follower. This provides software control of contrast and the absolute minimum component count. TABLE 1 provides the possible combinations of V_{DD} and DC-to-DC boost ratio. FIGURE 6 provides the boost capacitor configuration..

FIGURE 7 shows the typical hookup.

FIGURE 8 shows the external power supply option. Use this hookup for least flicker.

TABLE 1 –F-55472-SERIES DC BOOST BY V_{DD}-V_{SS}

PART NUMBER	1.8	2.2	2.5	2.8	3.0	3.3	3.6
F-55472GNFJ-SLW-AAN	EXT	EXT	EXT	INT 4X	INT 4X	INT 4X	INT 3X
F-55472GNFQJ-LW-ABN	EXT	EXT	EXT	INT 4X	INT 4X	INT 4X	INT 3X
F-55472GNBJ-LW-ACN	EXT	EXT	EXT	INT 4X	INT 4X	INT 4X	INT 3X
F-55472GNFQJ-LB-AEN	EXT	EXT	EXT	INT 4X	INT 4X	INT 4X	INT 3X
F-55472GNFQJ-LG-ADN	EXT	EXT	EXT	INT 4X	INT 4X	INT 4X	INT 3X

CAUTION:

DO NOT USE 4x BOOST WITH 3.6 V V_{DD}. THE BOOSTED VOLTAGE EXCEEDS THE MAXIMUM RATING FOR THE V_{OUT} PIN OF THE NT7534.

5.2.4. The NT7534 controls contrast via the ELECTRONIC VOLUME REGISTER (EVR) setting in software. The internal voltage regulator gain [(1+ (R_B / R_A)] sets the control range. The graphs at the end of this document provide optimal EVR settings with 3.0 V V_{DD} and a gain of 5.0 with either internal or external resistors. If V_{DD} <> 3.0 V, or a different gain is selected, the user must calculate the desired EVR setting from equation A-1 of reference (a) and confirm the DC / DC boost generates [VOUT > (V_0 - $V_{SS)}$ + 0.1 V]. The V_0 – V_{SS} value is found in Section 3.1 of the LCD Module Specification.

For users with F-55472 with external gain resistors, selecting R_A = 330 KΩ and R_B = 1.33 MΩ yields a gain of 5.0 and allows EVR setting to control contrast over the entire temperature range. This choice also meets the requirement of R_A + R_B > 1.5 MΩ.

V_0-V_{SS} from Table 3.1 of the display specification is the voltage drop across R_B and R_A. The current is (V_0 – V_{SS}) / (R_A + R_B).

5.2.5. Use the following values for the boost and bypass capcitors (see FIGURE 6 and FIGURE 7):

Boost capacitors (C1) – 1.0 µF to 4.7 µF, 16 V.

These are not required and may be left open if using an external power supply to V_0 to V_4. These pins may also be left open if supplying V_{OUT} from an external supply.

Bypass capacitors (C2) – 0.1 µF to 2.2 µF, 16 V. These capacitors are required.

The voltage differences between V_0-V_1, V_1-V_2, V_3-V_4 and V_4-V_{SS} should be equal. The magnitude is the bias voltage difference (see equations in FIGURE 5).

If the display has uneven pixel contrast, increase the size of the C2 capacitors to stabilize the voltage.

Determine the C2 value by displaying a heavy load image (such as horizontal stripes) and selecting a value that stabilizes the liquid crystal driven voltages (V_0 to V_4) and minimizes pixel color difference and flicker. Note that all capacitors must have the same capacitance value.

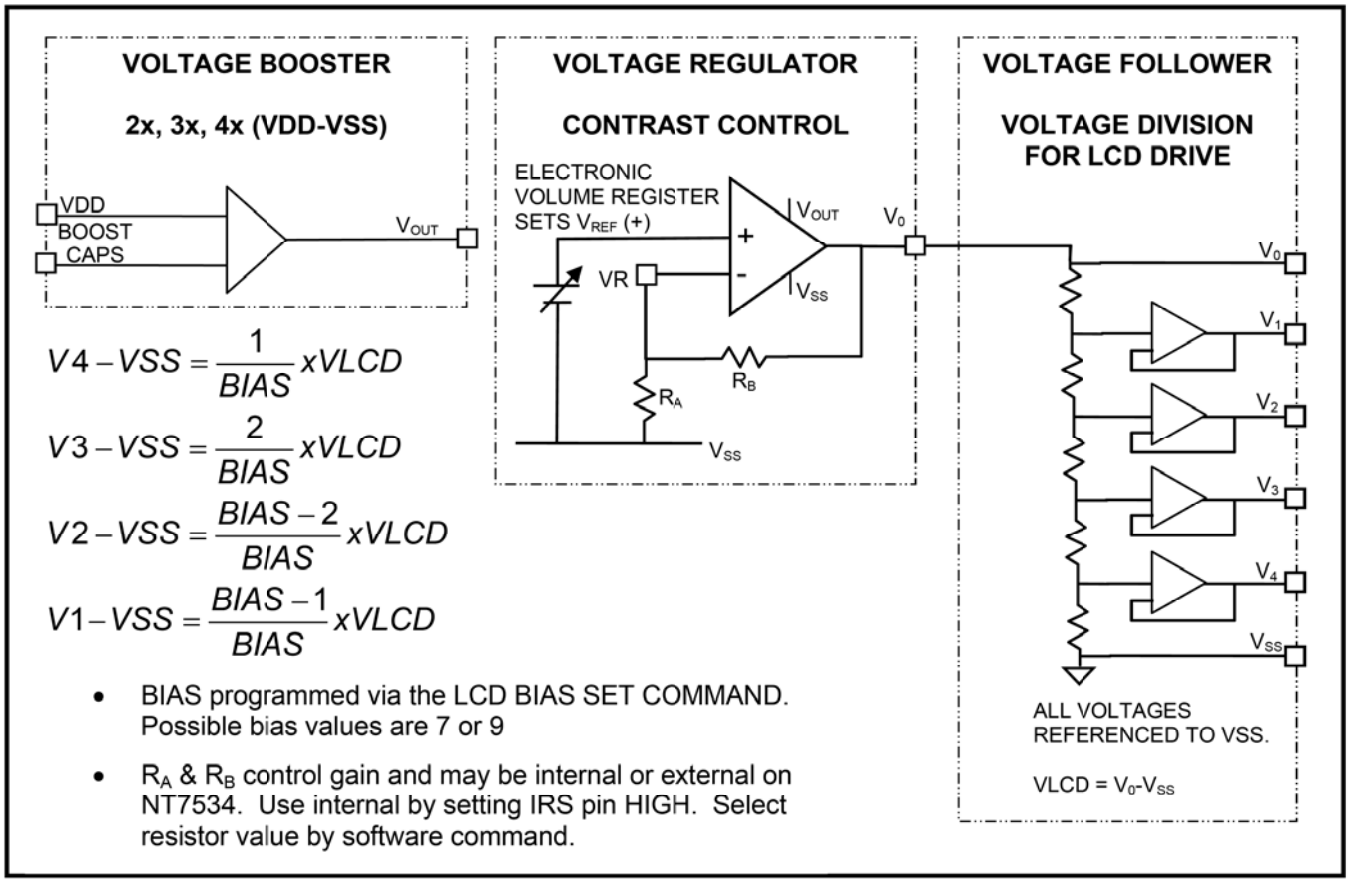
5.2.6. The F-55471 use two controllers in MASTER – SLAVE setup. The DC-to-DC boost is permanently disabled on the SLAVE. The MASTER does not have sufficient drive to run the display – an external power supply generating V_0 to V_4 supply for both ICs is required.

Optrex does not recommend using the internal voltage regulator and follower on the master to supply the slave.

IC Production variation between the master and slave will cause slight voltage differences and contrast variation by display quadrant. To avoid this phenomena, the voltage regulators

and dividers on the master and slave should not be used. Supply V_0 to V_4 from an external power supply to ensure equal voltages on both ICs.

FIGURE 5 – NT7534 LCD DRIVE CIRCUITRY



$$V4 - VSS = \frac{1}{BIAS} xVLCD$$

$$V3 - VSS = \frac{2}{BIAS} xVLCD$$

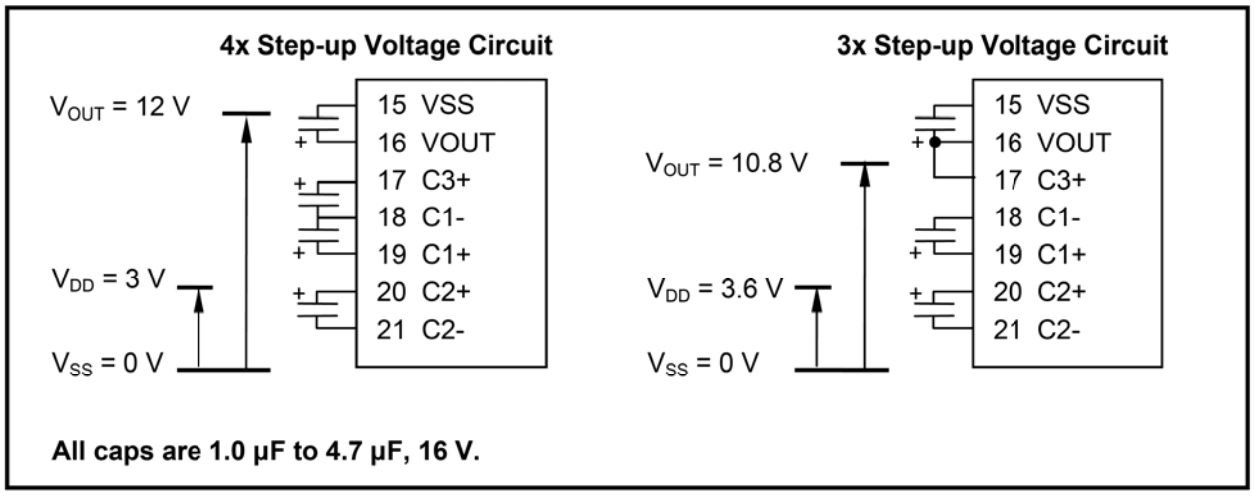
$$V2 - VSS = \frac{BIAS - 2}{BIAS} xVLCD$$

$$V1 - VSS = \frac{BIAS - 1}{BIAS} xVLCD$$

- BIAS programmed via the LCD BIAS SET COMMAND. Possible bias values are 7 or 9
- R_A & R_B control gain and may be internal or external on NT7534. Use internal by setting IRS pin HIGH. Select resistor value by software command.

5.2.7. VOLTAGE BOOST SETUP

FIGURE 6 – F-55472 VOLTAGE BOOST CONFIGURATION



All caps are 1.0 µF to 4.7 µF, 16 V.

FIGURE 7 – SETUP FOR DC BOOST, VOLTAGE REGULATOR & FOLLOWER

OPTION 1

4x DC to DC Boost Circuit ON
Voltage Regulator ON
Voltage Follower ON

Use Internal resistors for VREG op-amp

OPTION 2

DC to DC Boost Circuit OFF
Voltage Regulator ON
Voltage Follower ON

Use internal resistors for VREG op-amp

Supply VOUT from External Supply

OPTION 3

DC to DC Boost Circuit OFF
Voltage Regulator OFF
Voltage Follower OFF

Supply V0 to V4 with External Supply

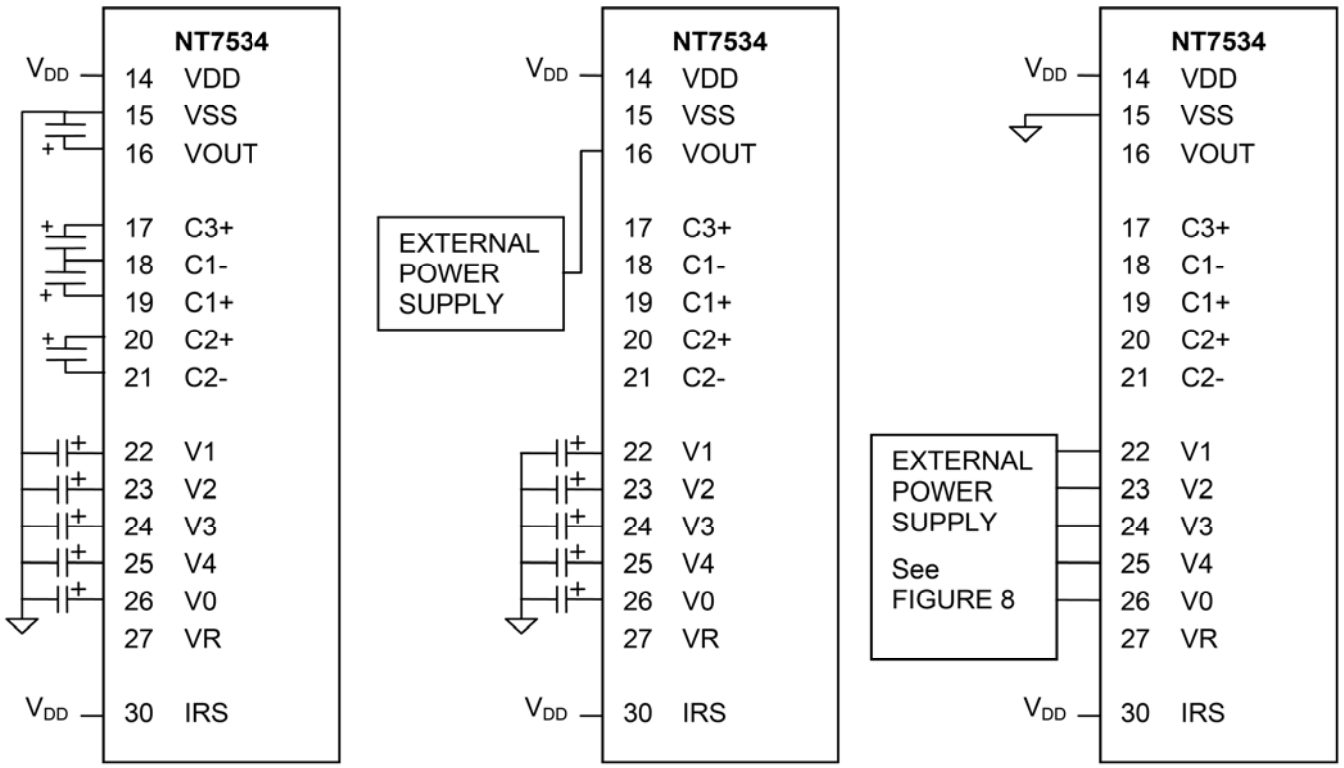


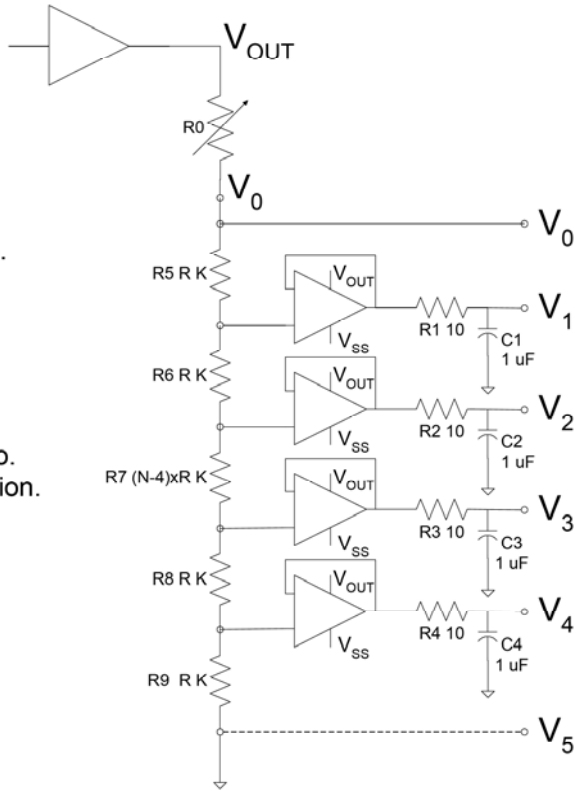
FIGURE 8 provides a reference design for an external power supply. In this configuration, the electronic volume control is physically bypassed and contrast control via software command is prevented. Display contrast is controlled by varying the magnitude of V_0. R5 through R9 generate the bias voltages. This power supply is required for F-55471 displays for both the master and slave.

Keep the traces between the outputs and the displays short. Long traces add resistance which creates voltage differences between the MASTER and SLAVE drive circuits which causes non-uniform contrast.

FIGURE 8 – F-55471 & F-55472, EXTERNAL POWER SUPPLY

NOTES

1. V_5 is connected internally within NT7534. It is shown here for information to aid understanding. V_5 is V_{SS}.
2. V_0 is a variable voltage. V_0 controls contrast.
   R0 is shown for functionality. V_0 is a variable voltage. R0 may be replaced with any voltage varying device desired.
3. The voltage drop across R7 is large. C2 must have adequate voltage rating.
4. The values of R5, R6, R8 and R9 are equal (R). R7 value is set by the bias ratio where N = 1 / BIAS Ratio. For N=9, R7 value is 5R. All resistors are 1 % precision.
5. Op amps are LM324 or equivalent.



5.3. SIGNAL TIMING

5.3.1. NT7534 timing varies with the operating voltage. 1.8 to 2.7 V_{DD} is slower than 2.7 to 3.6 V_{DD}. Please consult reference (a), AC Characteristics, if you intend to use V_{DD} other than that listed in the LCD module specification.

5.3.2. RESET duration is important; please follow the LCD module specification guidance. If RESET is not held low for the correct time, abnormal operation is possible.

5.3.3. If NT7534 hardware RESET is executed simultaneously with the microprocessor RESET, an overcurrent condition can occur if the microprocessor control signals enter the high impedance state.

5.3.4. The controller-driver instructions require time to execute. While instructions are executing, commands and data should not be sent.

The status of the controller can be read with a parallel interface by using the STATUS READ command to return the BUSY FLAG value. If the software design does not examine this bit, the T_{CYC} requirements must be met to ensure adequate time for the controller to act upon commands. It is not possible to read status via the SPI interface, so the T_{SCYC} must be met.

5.4. BACKLIGHT

5.4.1. The F-55471 and F-55472-series backlights use a JST PHR-2 connector. This is a removable, 2 mm pitch, crimp pin connector using the PHR-2 housing. The mating connector is a 2-pin header.

JST S 2B-PH-SM3-TB – 2-pin, surface mount, side entry, shrouded header, 2 mm pitch.

5.4.2. The mechanical drawing backlight schematic shows resistors; these are populated with zero ohm values. The designer must limit drive current.

If using a current limiting resistor must meet the criteria of EQUATION 1 and have adequate power rating.

EQUATION 1 – CURRENT LIMITING RESISTOR CALCULATION

$$\frac{V_{SUPPLY} - V_F}{R} \leqslant I_F$$

The values of V_F and I_F are found in Section 2.4. of the LCD Module Technical Specification for the F-55472 and Section 2.5 for the F-55471. PWM techniques may be used to control luminance. The high temperature current deratings must be followed.

5.5. POWER SUPPLY SEQUENCING & SIGNAL TRANSIENTS

5.5.1. The external power supply should be sequenced so that the voltage comes up after V_{DD} at startup and shuts down before V_{DD} at power down. This sequencing should be maintained for inadvertent power down as well.

5.5.2. When supplying VLCD externally, the RESET pin should be held LOW while powering on the VLCD supply for V_0 to V_4.

5.5.3. The backlight drive voltage should be energized after the LCD is configured and placed in operation to hide optical effects caused by startup with undefined data in the RAM. Likewise, the backlight should be powered OFF before the the display during shutdown.

6.0 SOFTWARE

6.1. Each data bit of RAM corresponds to pixel location in the display. This means the display can generate monochrome images by setting the value of a data bit to 1 or 0.

The RAM is organized into 8-bit tall “pages” corresponding to the commons (horizontal lines) on the display. An 8-bit data write maps to eight pixels in a vertical column. A specific RAM location is selected by specifying the PAGE ADDRESS SET to specify the vertical location and the COLUMN ADDRESS SET to specify the horizontal location.

Reference (a) pages 15 and 16 discuss NT7534 RAM operation. The mapping of pixels to RAM is shown in FIGURE 9 and FIGURE 10.

6.2. The procedure for writing to the display is:

Execute a PAGE ADDRESS SET to specify the 8-bit vertical location of the data write.

Execute a COLUMN ADDRESS SET to specify the horizontal location.

Execute a DATA WRITE command. The RAM pointer increments automatically.

Execute additional data writes until the RAM reaches the end of a line.

Set the PAGE ADDRESS SET and COLUMN ADDRESS SET as needed to continue. The COLUMN ADDRESS SET must be executed, as the pointer does not automatically reset upon reaching the end of the line.

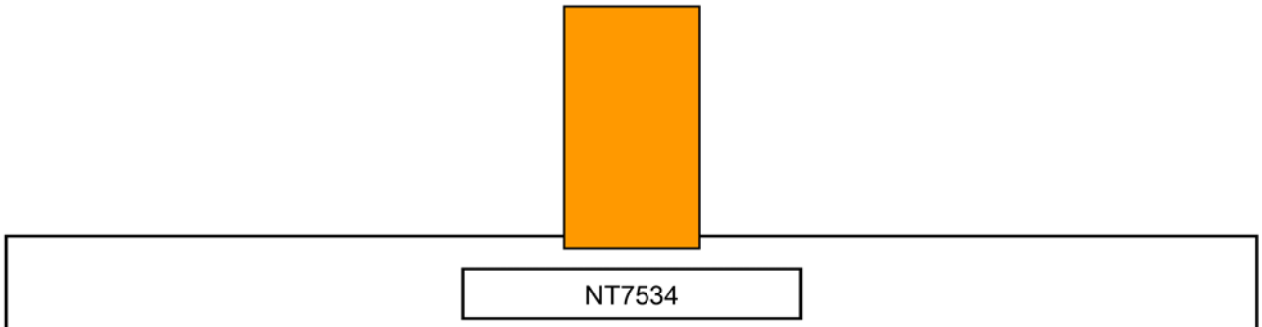
The ADC SET command controls the direction of the RAM write.

Given the pixel mapping of FIGURE 9, a left to right and up to down image scan requires setting the ADC SELECT register value to $0xA1 to reverse the horizontal scan and the COMMON OUTPUT MODE SELECT register value to $0xC8 to reverse the vertical scan.

6.3. Unused RAM locations in the NT7534 may be used for scratchpad memory. Unused RAM locations are:

- PAGES 1 to 7 Column Addresses $0x80 to $0x83 (ADC = 1) or $0x00 to $0x02 (ADC = 0)
- PAGE 8. These single bits control icons, which are not implemented in the display.

FIGURE 9 – F-55472 PIXEL TO RAM MAPPING & ITO CONNECTIONS



PIXEL 0, 0
SEG131 COLUMN ADDRESS 0x00 (ADC = 1, L TO R RAM WRITE)
SEG131 COLUMN ADDRESS 0x83 (ADC = 0, R TO L RAM WRITE)
COM0 Line Address 00H (BIT 0) PAGE ADDRESS SET 0xB0

PIXEL 127, 0
SEG4 COLUMN ADDRESS 0x7F (ADC = 1, L TO R RAM WRITE)
SEG4 COLUMN ADDRESS 0x04 (ADC = 0, R TO L RAM WRITE)
COM0 Line Address 00H (BIT 0) PAGE ADDRESS SET 0xB0

DISPLAY AREA 128 x 64 PIXELS

PIXEL 0, 63
SEG131 COLUMN ADDRESS 0x00 (ADC = 1, L TO R RAM WRITE)
SEG131 COLUMN ADDRESS 0x83 (ADC = 0, R TO L RAM WRITE)
COM63 Line Address 3F H (BIT 7) PAGE ADDRESS SET 0xB7

PIXEL 127, 63
SEG4 COLUMN ADDRESS 0x7F (ADC = 1, L TO R RAM WRITE)
SEG4 COLUMN ADDRESS 0x04 (ADC = 0 R TO L RAM WRITE)
COM63 Line Address 3FH (BIT 7) PAGE ADDRESS SET 0xB7

FIGURE 10 -- F-55471 PIXEL TO RAM MAPPING & ITO CONNECTIONS

PIXEL 1, 1 SEG131 Column Address 0x00 COM0 Line Address 0x00	**PIXEL 132, 1** SEG0 Column Address 0x83 COM0 Line Address 0x00
Quadrant 1 – MASTER segments & SLAVE commons	
PIXEL 1, 32 SEG131 Column Address 0x00 COM32 Line Address 0x1F	**PIXEL 132, 32** SEG0 Column Address 0x83 COM32 Line Address 0x1F
PIXEL 1, 33 SEG131 Column Address 0x00 COM33 Line Address 0x20	**PIXEL 132, 33** SEG0 Column Address 0x83 COM33 Line Address 0x20
Quadrant 3 – MASTER segments & MASTER commons	
PIXEL 1, 64 SEG131 Column Address 0x00 COM64 Line Address 0x3F	**PIXEL 132, 64** SEG0 Column Address 0x83 COM64 Line Address 0x3F

PIXEL 133, 1 SEG131 Column Address 0x00 COM0 Line Address 0x00	**PIXEL 240, 1** SEG24 Column Address 0x18 COM0 Line Address 0x00
Quadrant 2 – SLAVE segments & SLAVE commons	
PIXEL 133, 32 SEG131 Column Address 0x00 COM32 Line Address 0x1F	**PIXEL 240, 32** SEG24 Column Address 0x18 COM32 Line Address 0x1F
PIXEL 133, 33 SEG131 Column Address 0x00 COM33 Line Address 0x20	**PIXEL 240, 33** SEG24 Column Address 0x18 COM33 Line Address 0x20
Quadrant 4 – SLAVE segments & MASTER commons	
PIXEL 133, 64 SEG131 Column Address 0x00 COM64 Line Address 0x3F	**PIXEL 240, 64** SEG24 Column Address 0x18 COM64 Line Address 0x3F

NOTE

Column addresses are based on left to right scan (ADC= 1)

6.4. SOFTWARE CONFIGURATION

Turn on $V_{DD} - V_{SS}$ while holding the RESET pin low. If supplying VLCD externally or supplying a voltage to the V_{OUT} pin, hold RESET low until all voltages stabilize. Note the power supply sequencing requirements for V_{DD}, V_{SS} and external voltages must be met.

Set RESET pin high. IC is initialized to default state.

Configure the IC with the following commands:

TABLE 2 – SOFTWARE CONFIGURATION COMMANDS

ITEM	COMMAND NAME	VALUE	COMMENT
1.	LCD BIAS SET	0xA2	Set LCD bias to 1/9 0xA2 1/9 bias 0xA3 1/7 bias
2.	ADC SELECT	0xA1	Inverse scan (L to R) 0xA0 Normal Scan R to L 0xA1 Inverse Scan L to R
3.	OUTPUT STATUS SELECT	0xC0	Scan commons top to bottom 0xC0 Normal scan top to bottom 0xC8 Inverse scan bottom to top
4.	DISPLAY START LINE SET	0x40	Start COM scan at line address 00H 0x7F start COM scan at line 3FH Use this for scrolling
5.	OSCILLATION FREQUENCY SELECT	0xE4	Set internal oscillator frequency f_{OSC}. 0xE4 31.4 KHz 0xE5 26.3 KHz
6.	DC / DC CLOCK FREQUENCY	0xE6	Enable DC boost clock setting.
7.	DC / DC FREQUENCY DIVISION SET	0x03	Set frequency of boost clock to f_{OSC} / 6. This command must follow immediately after DC / DC clock set command. No other commands are accepted in this position.
8.	N-LINE INVERSION SET	0x85	Enable N-Line voltage inversion.
9.	N-LINE INVERSION NUMBER OF LINE SET	0x0A	Set number of lines + 1 = 11. This command must follow immediately after DC / DC clock set command. No other commands are accepted in this position. Change the value of this register if partial display mode used.
10.	V_0 VOLTAGE REGULATOR INTERNAL RESISTOR RATIO	0x25	0x25 for $(1+ (R_B/R_A)) = 5.0$ Use to set value of internal resistor ratio for electronic voltage regulator amplifier.

ITEM	COMMAND NAME	VALUE	COMMENT
	SET		
11.	ELECTRONIC VOLUME MODE SET	0x81	Access the electronic volume register
12.	ELECTRONIC VOLUME REGISTER SET	0x**	Set value of EVR to control contrast. Obtain values from graphs on pages 20 to 23. If V_{DD} <> 3.0 V, or a different gain is selected, the user must calculate the desired EVR setting from equation A-1 of reference (a) and confirm the DC / DC boost generates VOUT > V_0 + 0.1 V.
13.	POWER CONTROL SET	0x2F	**FIGURE 7 OPTION 1 – Recommended for F-55472** DC-to-DC Boost ON, Voltage Regulator ON, Voltage Follower ON to provide software control of contrast. **[FIGURE 7 OPTION 2 EXTERNAL V_{OUT}]** 0x2B to set DC-to-DC Boost OFF, Voltage Regulator ON, Voltage Follower ON. **[FIGURE 7 OPTION 3 EXTERNAL POWER SUPPLY]** $0x28 to set DC-to-DC Boost OFF, Voltage Regulator OFF, Voltage Follower OFF. These functions are performed by external power supply.
14.	ENTIRE DISPLAY ON	0xA4	Normal display 0xA5 to turn on all pixels by overriding contents of RAM. RAM not affected. Use for testing. When display is turned OFF with the DISPLAY ON / OFF commnad (0xAE), Set ENTIRE DISPLAY ON to 0xA5 to enter power save mode.
15.	DISPLAY ON / OFF	0xAF	Display ON 0xAE display OFF. Use to control Power save mode with ENTIRE DISPLAY ON command. 0xAF display ON
16.	PAGE ADDRESS SET	0xB0	Select RAM page 0 to start writing at pixel 0 vertically.
17.	COLUMN ADDRESS SET	0x10	Set upper 4 bits of column starting address to 00H.
18.	COLUMN ADDRESS SET	0x00	Set lower 4 bits of column starting address to 00h. Display is now ready to begin RAM write at pixel 0, 0 in upper left

ITEM	COMMAND NAME	VALUE	COMMENT
			corner and scan left to right.
19.	WRITE DISPLAY DATA	0x**	data to be displayed. RAM column (horizontal) address will auto increment with each write. Reset column at end of horizontal row.

6.5. CONTROLLER / DRIVER CONFIGURATION & COMMISSIONING

6.5.1. Over time, commands to the controller may be corrupted by conducted or emitted noise (EMI) or electro-static discharges (ESD). The NT7534 does not use error detection and correction techniques to identify invalid commands. Using an invalid command may cause the controller to enter an undefined state. Periodically, a hardware RESET should be commanded to ensure a baseline configuration is attained. Follow up the RESET with a complete configuration and data image to ensure proper operation.

6.5.2. Execute the software RESET command ($0xE2) more frequently than the hardware RESET to ensure proper configuration of the controller. Software RESET does not affect the data image but does require register initialization.

In the software RESET sequence, add the TEST MODE RESET command ($0xF0). TEST MODE RESET clears an inadvertent issue of the TEST MODE command caused by EMI.

6.5.3. During initial development, Optrex recommends using a parallel data interface, which allows reading the NT7534 status and RAM. The STATUS READ command returns the BUSY FLAG condition which is used to determine if the microprocessor is communicating with the controller and whether the controller able to accept data/commands. This feature is useful during development for confirming that EMI or ESD are not corrupting data by looking for a busy flag that does not clear within T_{CYC} or an active RESET flag. Once stability is demonstrated, the busy flag check may be removed.

Alternative methods for confirming correct communication are:

- Execute an ELECTRONIC VOLUME SET command and verify the voltage on V_0 changes as expected. An A/D converter is required.
- Perform a data write and then execute a data read to confirm receipt. This is not possible with SPI interface.
- Execute a READ STATUS command (not possible with SPI interface).

6.5.4. The controller instructions require time to execute (T_{CYC}). While instructions are executing, commands and data should not be sent as the NT7534 ignores commands while busy. The BUSY FLAG status is read by using the STATUS READ command. If the software design does not examine this bit, such as in SPI interface, the T_{CYC} requirements must be met to ensure adequate time for command execution. T_{CYC} defines the fastest data rate between the host and the display.

Please note that the system cycle time varies with logic voltage.

6.5.5. The fastest RAM image update rate, T_{CYC}, is significantly faster than the liquid crystal response speed. There are two liquid crystal response speeds: T_{RISE} and T_{FALL}, whose values are given in Section 3.2 of the LCD module specification. A typical total response time is 110 mS T_{RISE} and 190 mS T_{DECAY}. Writing to the display with data that alternates state (1…0…1…0…) to the same RAM location will cause the pixel to not achieve the full ON or OFF light transmittance level. Contrast ratio will decrease and the image may appear fuzzy.

To achieve full contrast ratio performance, the image data should not be updated faster than the rate defined by

$$\text{MAX Image Update Rate for Full Contrast} = \frac{2}{T_{RISE} + T_{FALL}}$$

For the data above, this rule of thumb suggests the image change rate is 2 / 0.300 S = 6.66 video frames per second.

Faster image update is possible, but contrast performance will be sacrificed. Also, the fastest typical human response speed is 215 mS[1] to read, recognize and react upon information change. This suggests a maximum video rate of 4 image changes per second.

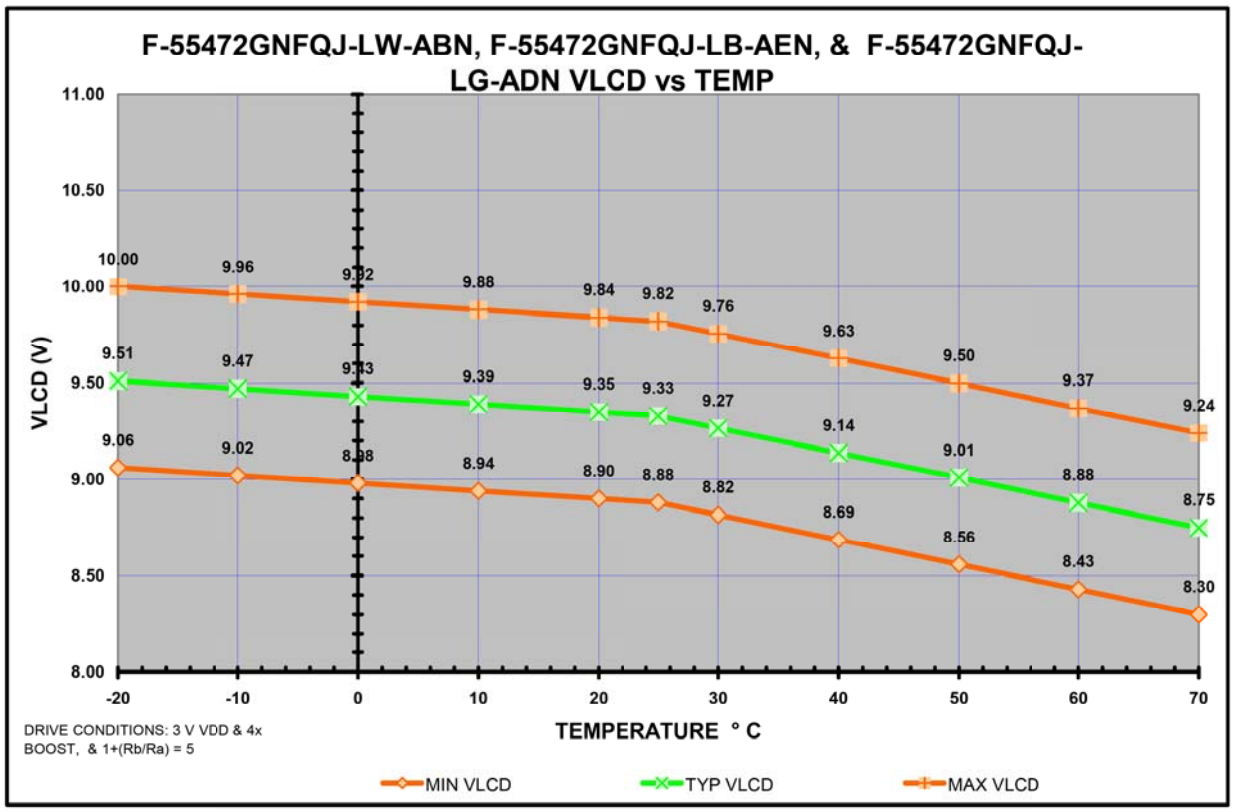
6.6. RECOMMENDED ELECTRONIC VOLUME REGISTER SETTINGS FOR CONTRAST CONTROL

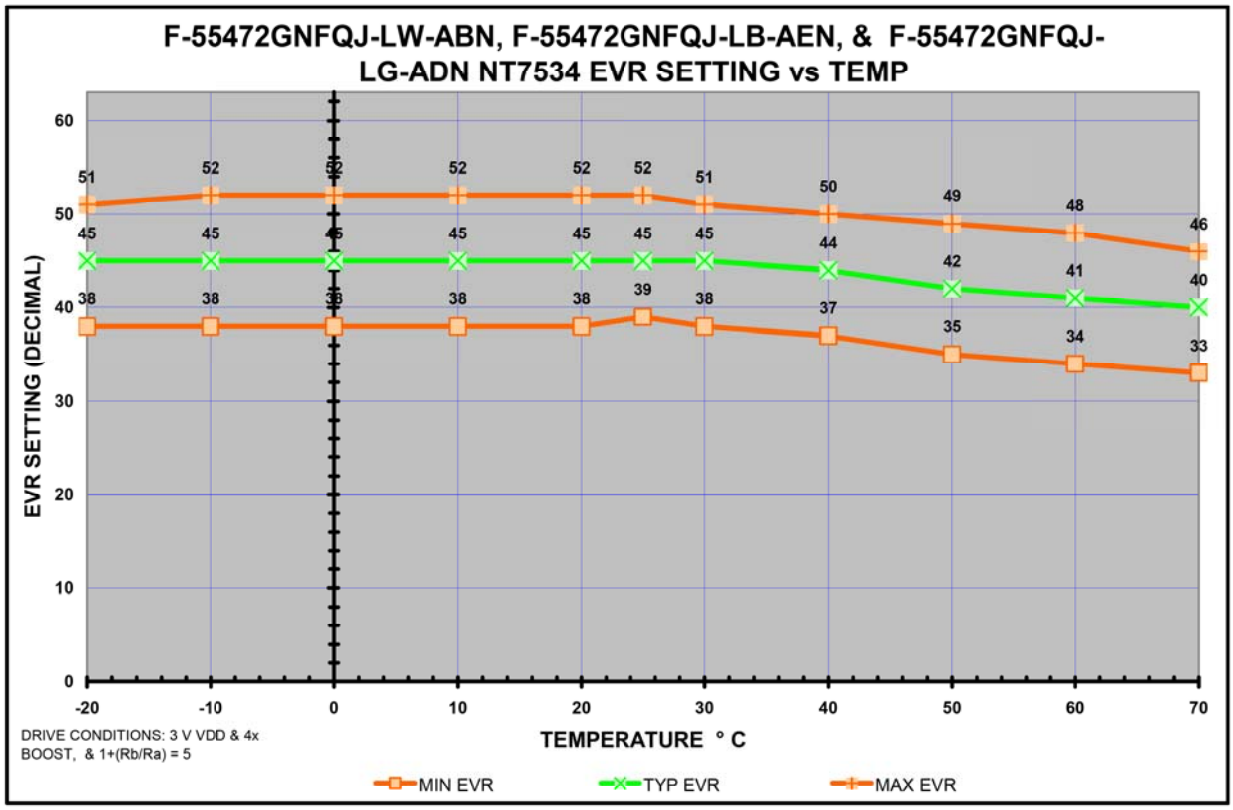
6.6.1. The following figures on pages 20 through 23 show the relationship between VLCD and temperature for proper contrast as well as ELECTRONIC VOLUME SET and temperature. Please note drive conditions in the lower left corner. These settings were calculated. If the $(1 + (R_B / R_A))$ amplification ratio is varied, the results will differ.

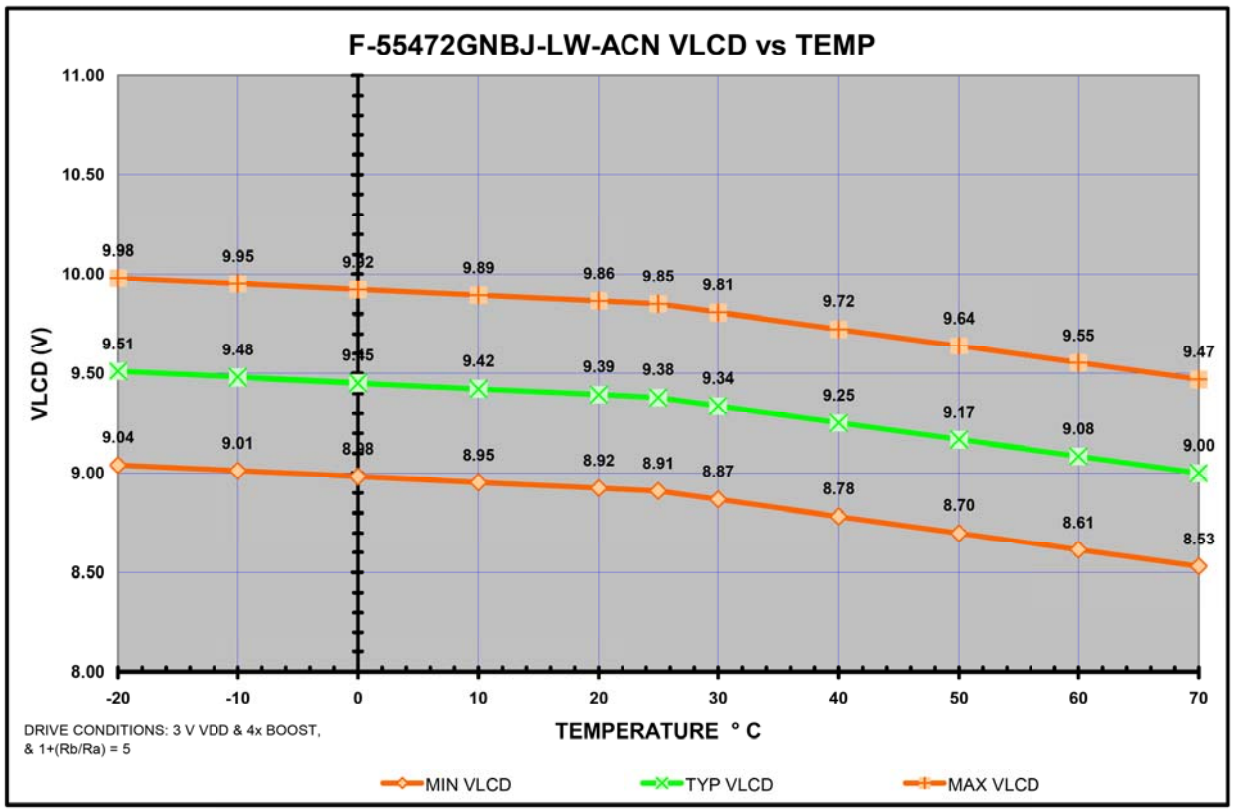
6.6.2. The EVR graphs are the production variation limits. Most displays will have an optimal setting much narrower than the range suggested by these graphs (see FIGURE 2 for an explanation). A robust system design and production process accomodates this variation by:

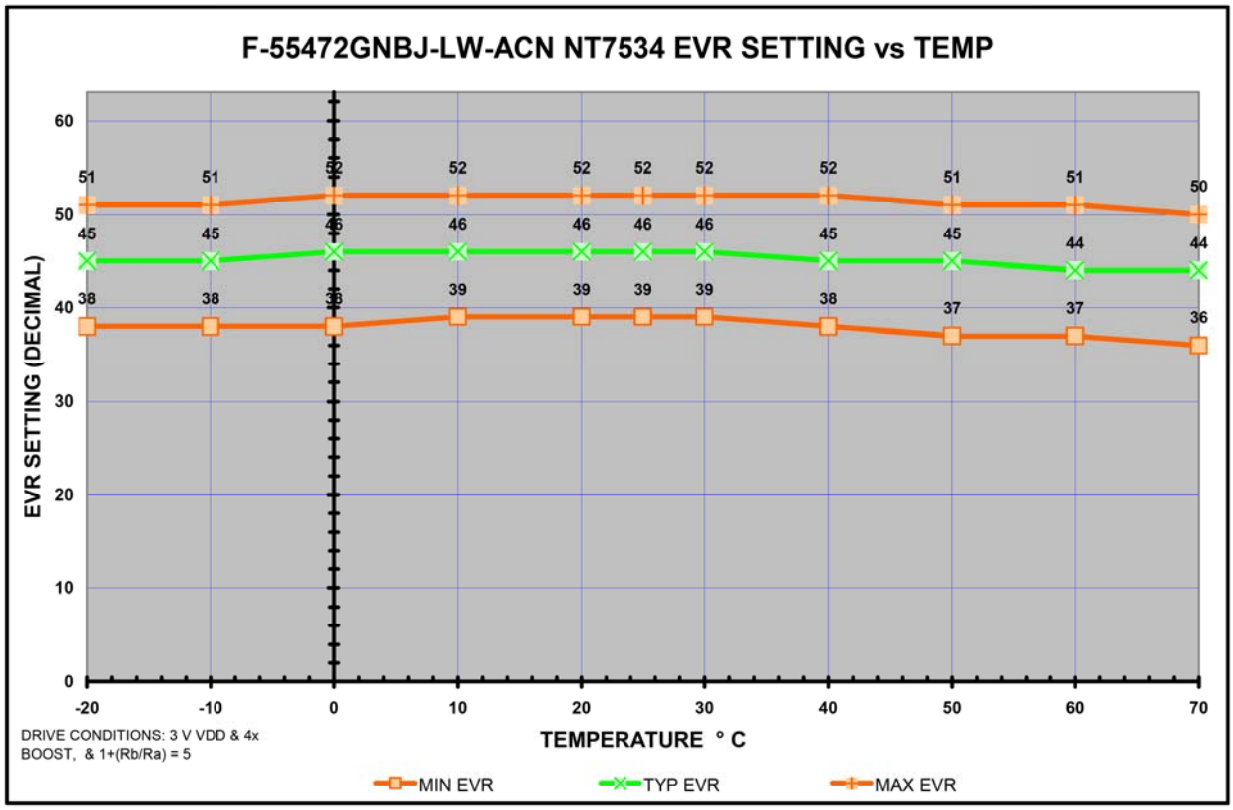
- Retaining the optimal 25° C EVR setting in memory. This value is set at the factory. This reduces optical variation and ensures all displays have similar appearance.
- Limits the low EVR setting to prevent adjusting the pixel voltage too low (all pixels OFF condition – no image). This setting prevents customers from adjusting to a point where they cannot see an image.
- Limits the high EVR setting to prevent adjusting the pixel voltage too high (all pixels ON condition – no image). This setting prevents customers from adjusting to a point where they cannot see an image.

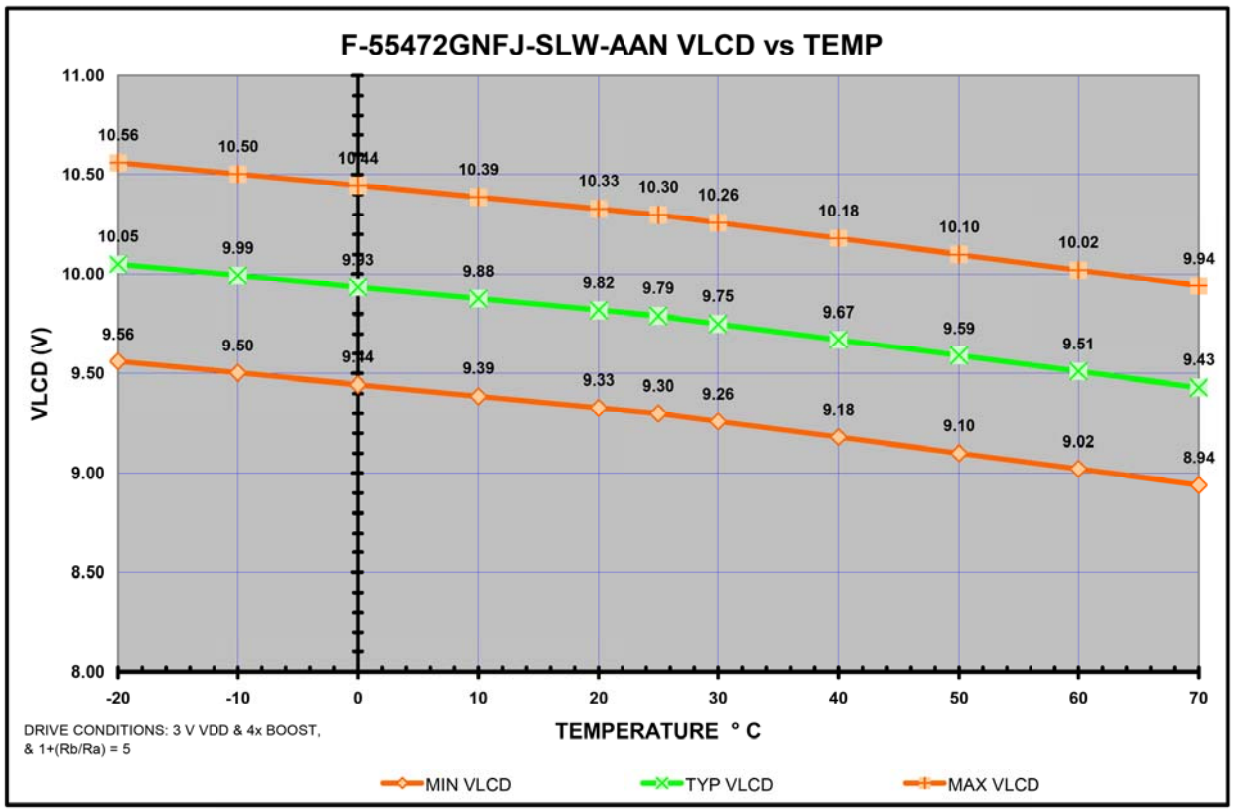
[1] http://www.humanbenchmark.com/tests/reactiontime/index.php

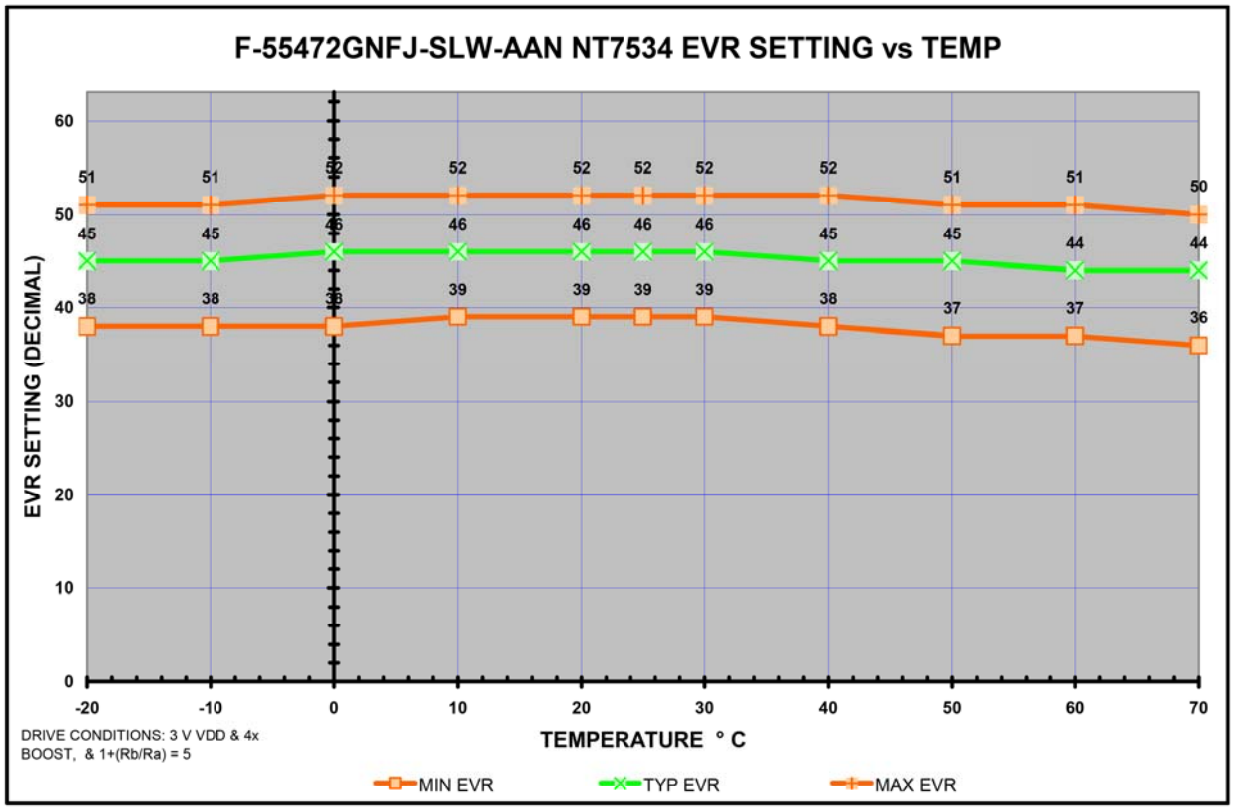

F-55472GNFQJ-LW-ABN, F-55472GNFQJ-LB-AEN, & F-55472GNFQJ-LG-ADN VLCD vs TEMP
VLCD (V)
TEMPERATURE ° C
DRIVE CONDITIONS: 3 V VDD & 4x BOOST, & 1+(Rb/Ra) = 5
MIN VLCD
TYP VLCD
MAX VLCD

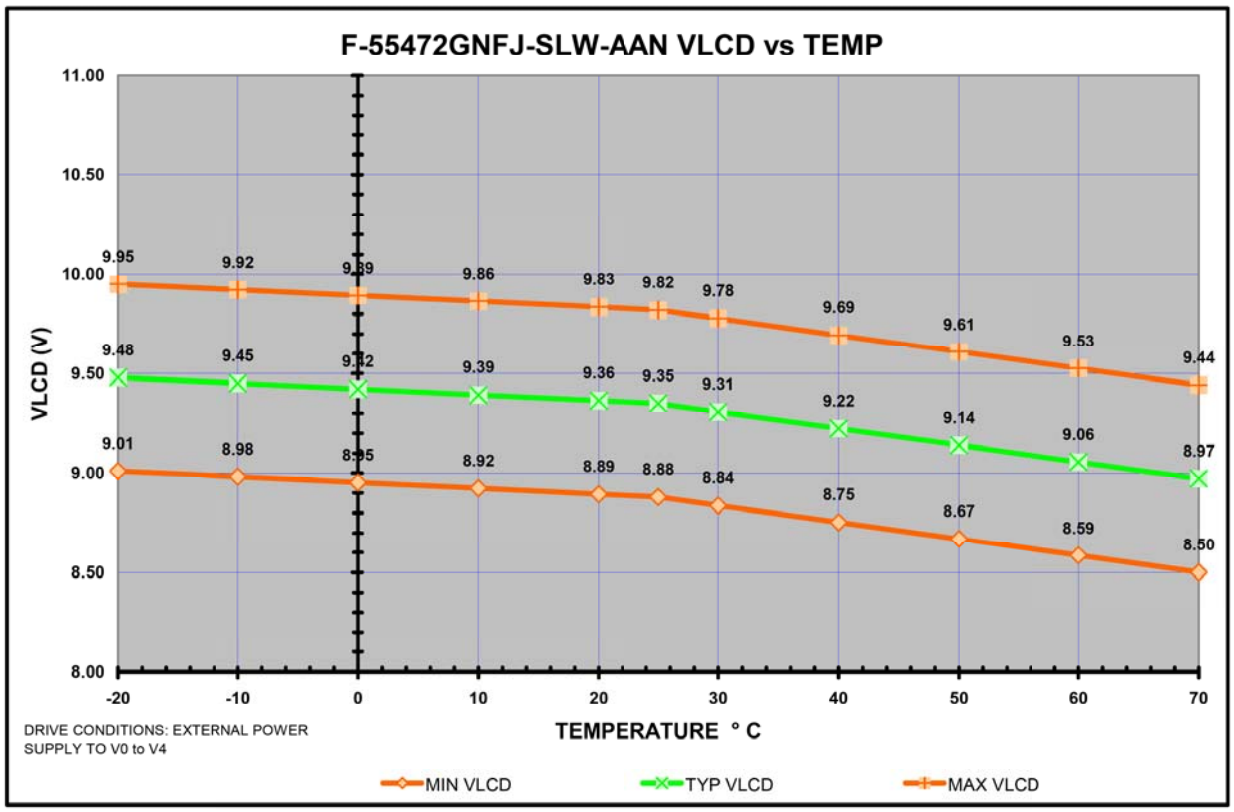

F-55472GNFQJ-LW-ABN, F-55472GNFQJ-LB-AEN, & F-55472GNFQJ-LG-ADN NT7534 EVR SETTING vs TEMP
EVR SETTING (DECIMAL)
TEMPERATURE ° C
DRIVE CONDITIONS: 3 V VDD & 4x BOOST, & 1+(Rb/Ra) = 5
MIN EVR
TYP EVR
MAX EVR

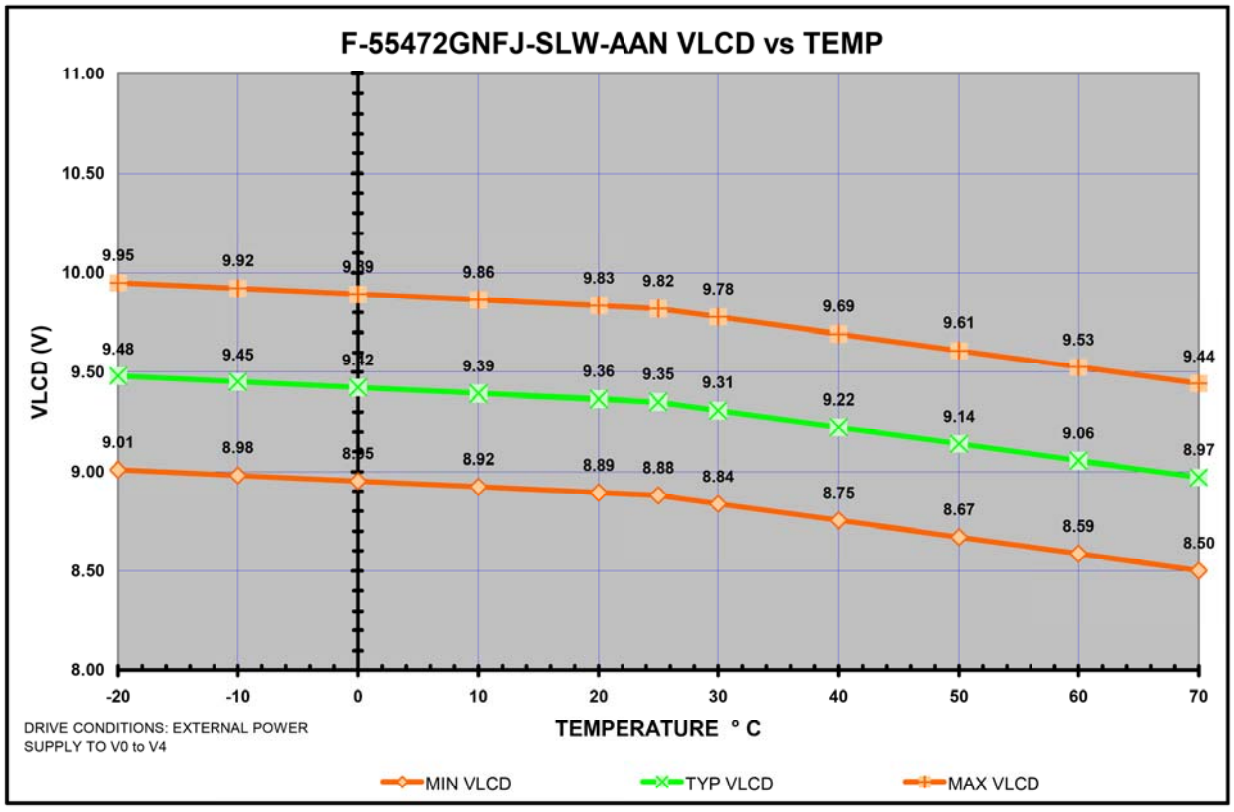

F-55472GNBJ-LW-ACN VLCD vs TEMP
VLCD (V)
TEMPERATURE ° C
DRIVE CONDITIONS: 3 V VDD & 4x BOOST, & 1+(Rb/Ra) = 5
MIN VLCD
TYP VLCD
MAX VLCD


F-55472GNBJ-LW-ACN NT7534 EVR SETTING vs TEMP
EVR SETTING (DECIMAL)
TEMPERATURE ° C
DRIVE CONDITIONS: 3 V VDD & 4x BOOST, & 1+(Rb/Ra) = 5
MIN EVR
TYP EVR
MAX EVR


F-55472GNFJ-SLW-AAN VLCD vs TEMP
VLCD (V)
TEMPERATURE ° C
DRIVE CONDITIONS: 3 V VDD & 4x BOOST, & 1+(Rb/Ra) = 5
MIN VLCD
TYP VLCD
MAX VLCD


F-55472GNFJ-SLW-AAN NT7534 EVR SETTING vs TEMP
EVR SETTING (DECIMAL)
TEMPERATURE ° C
DRIVE CONDITIONS: 3 V VDD & 4x BOOST, & 1+(Rb/Ra) = 5
MIN EVR
TYP EVR
MAX EVR





This bookmark indicates last page of graphs.

7.0 HANDLING RECOMMENDATIONS

7.1. FPC HANDLING PRECAUTIONS

- DO NOT pick the display up by the FPC tail. This action can break the electrical connection to the glass or peel the FPC away.
- DO NOT PULL the FPC. This action can break the electrical connection to the glass or peel the FPC away.
- DO NOT BEND THE FPC UPWARD from the glass surface. This will break the electrical connection to the glass.
- DO NOT BEND THE FPC TIGHT and form creases. This will fracture the copper traces and cause an open circuit.
- ALWAYS bend the FPC so the bend applies a compressive force to the FPC to GLASS bond area.

7.2. LCD PROTECTIVE LINER

- Optrex manufactures the display with an optical-grade, clear protective liner attached to the front polarizer. The liner is optical grade; allowing display visual inspection while attached.
- Leave the liner installed until the last possible moment in production to protect the polarizer from impact scratches, fingerprints, and airborne debris.
- Remove the protective liner by placing a small piece of adhesive tape at a corner and press it in place. SLOWLY use the tape to pull the protective liner up and roll off the glass. The protective liner should bend 180° back upon itself as it is slowly pulled. A slow pulling speed reduces electrostatic voltage activating the pixels.

8.0 PROTOTYPING RECOMMENDATIONS

8.1. The display interface is via ZIF connector making it difficult to construct hand-built prototypes. A source for ZIF to wire breakouts for prototyping is Quadrangle Products.

8.2. Adapter part numbers for F-55472 are:

Quadrangle RT-700G-30-DIS – 30 Conductor, 0.5 mm pitch, FPC to discrete wire adapter.

Quadrangle QD7018C – 30 Conductor, 0.5 mm pitch, female-to-female ZIF adapter. This product plugs into the display ZIF and RT-700G-30-DIS converting 30 conductors, 0.5 mm pitch FPC to discrete wire.

8.3. Quadrangle does not make a 36-pin adapter. You must use a 45-pin adapter and position the flex against one side leaving nine pins not connected. Adapter part numbers for F-55471 are:

Quadrangle RT-700G-45-DIS – 45 Conductor, 0.5 mm pitch, FPC to discrete wire adapter.

Quadrangle QD7018-45C – 45 Conductor, 0.5 mm pitch, female-to-female ZIF adapter. This product plugs into the display ZIF and RT-700G-30-DIS converting 45 conductors, 0.5 mm pitch FPC to discrete wire.

9.0 TRANSITION FROM F-51852-SERIES DISPLAYS to F-55472-SERIES

9.1. The F-55472 has the same mechanical size and fit as the F-51852-series thin displays (6.0 mm thick). Optrex will not produce a thick version (11.8 mm thick) of F-55472.

9.2. The F-51852-series displays mount an NJU6676 controller driver. This IC is negatively biased so that V_1 to V_5 voltages are relative to V_{DD}. The V_1 to V_5 voltages are negative.

$V_{DD} > V_1 > V_2 > V_3 > V_4 > V_5 > V_{OUT}$.

The NT7534 is positively biased and all voltages are relative to VSS. This means The V_1 to V_5 voltages are now positive.

$V_{OUT} > V_0 > V_1 > V_2 > V_3 > V_4 > V_{SS}$

The different voltage definition requires board layout changes even though the F-55472 signal names match the F-51852.

9.3. CN1 Connector Changes

TABLE 3 – F-51852 TO F-55472 CN1 INTERFACE CHANGES

PIN	F-51852 NAME	F-55472 NAME	FUNCTION	F-51852 to F-55472 DESIGN CHANGE	CUSTOMER DESIGN CHANGE
16	V_{OUT}	V_{OUT}	DC / DC Boost Circuit Output External DC / DC Boost Input	Voltage polarity change.	If Internal DC / DC Boost Used Change bypass cap routing from V_{DD} to V_{SS} to match FIGURE 7 OPTION 1. If External DC / DC Boost Used Consider change to use Internal DC / DC boost and reduce component count. If will continue to use external boost, change voltage polarity and magnitude. See FIGURE 7 OPTION 2.
17	C3-	C3+	DC / DC Boost Cap Connection.	Voltage polarity	IF DC / DC Boost Used: Rotate electrolytic capacitor polarity to match FIGURE 7 OPTION 1. No change non-polarized capacitor used. IF DC / DC Boost Not Used: Leave no-connected.
18	C1+	C1-			
19	C1-	C1+			
20	C2-	C2+			
21	C2+	C2-			
22	V_1	V_1	Voltage Follower Output External Voltage Supply Input	Voltage polarity & magnitude change. F-51852 – 1/9 x (V_{DD}-V_5). F-55472 – 8/9 x (V_0-V_{SS})	If Voltage Follower Used: Confirm capacitor voltage rating. Change capacitor bypass routing from V_{DD} to V_{SS} to match FIGURE 7 OPTION 1 or OPTION 2. Rotate electrolytic capacitor polarity (if applicable). If External Power Supply Used Change external power supply circuit to match FIGURE 8. Connect to display per FIGURE 7 OPTION 3.
23	V_2	V_2		Voltage polarity & magnitude change F-51852 – 2/9 x (V_{DD}-V_5). F-55472 – 7/9 x (V_0-V_{SS})	
24	V_3	V_3		Voltage polarity & magnitude change F-51852 – 7/9 x (V_{DD}-V_5). F-55472 – 2/9 x (V_0-V_{SS})	
25	V_4	V_4		Voltage polarity & magnitude change F-51852 – 8/9 x (V_{DD}-V_5). F-55472 – 1/9 x (V_0-V_{SS})	
26	V_5	V_0		Voltage polarity & magnitude change LCD driving voltage magnitude (V_0-V_{SS}) is lower due to new liquid crystal. F-51852 – V_5 is large negative voltage. F-55472 – V_0 is large, positive voltage.	
27	VR	VR		Voltage polarity & magnitude change	
30	NC	IRS	F-51852 – no connect F-55472 – select	Add internal voltage gain resistors.	Pull the pin to V_{DD} to use internal resistors. Delete the external resistors connecting to the VR pin

PIN	F-51852 NAME	F-55472 NAME	FUNCTION	F-51852 to F-55472 DESIGN CHANGE	CUSTOMER DESIGN CHANGE
			internal / external gain resistors for voltage regulator.		Set Register R17 V_0 VOLTAGE REGULATOR INTERNAL RESISTOR RATIO SET value in software per Section 6.6.

9.4. AC & DC Characteristics

9.4.1. The F-51852 supports 1.8 to 5 V V_{DD}. The F-55472 allows 1.8 to 3.6 V V_{DD}. 5 V operation is no longer possible.

The maximum V_{DD} and amount of DC to DC boost are related. With 4x boost, the maximum V_{DD} is 3.3 V. With 3.6 V V_{DD}, the maximum DC boost factor is 3.

The DC power consumption for the logic portion decreases from 5.3 mW to 3.6 mW.

The backlight power characteristics remain unchanged for the various color choices.

9.4.2. Timing characteristics vary by V_{DD}. The ranges are 1.8 to 2.7 V and from 2.7 to 3.6 V.

The AC characteristcs of NT7534 are slightly faster than NJU6676. The system cycle time, T_{CYC} reduces from 300 nS to 240 nS for both 68- and 80-series MPU at 2.5 to 3.3 V. The enable or control pulse for write operations increases from 60 nS to 90 nS.

9.5. The F-55472 uses a different liquid crystal fluid than F-51852. This new fluid has a lower voltage requirement enabling reduced component count by using the internal power circuits of the NT7534. An external DC boost circuit supplying the V_{OUT} pin is not required. There are slight changes in contrast ratio and viewing cone. The response time is significantly faster.

9.6. The NT7534 software commands mimic the NJU6676, but incorporates more features for improved performance. Software that worked for F-51852 will generate images with F-55472 but may not have optimum performance. TABLE 2 shows the configuration commands for NT7534. The commands 5 through 9 are NT7534-specific and should be added to the initialization routines written for the NJU6676.

The LCD DRIVER ON / OFF command (0xE7) is not implemented in the NT7534. Remove this command from software code.

The electronic volume register settings require updating.

10.0 TRANSITION FROM F-51851-SERIES DISPLAYS to F-55471-SERIES

10.1. The discussion of sections 9.2, 9.4, 9.5, and 9.6 apply to the F-51851 to F-55471 transition.

10.2. The F-55471 pinout for CN1 and CN2 differs from the F-51851 from pins 23 to 36. They are shifted by one position.

Table 4 – F-51851 TO F-55471 CN1, CN2 INTERFACE CHANGES

F-51851 PIN	F-51851 NAME	F-55471 PIN	F-55471 NAME	FUNCTION	F-51851 to F-55471 DESIGN CHANGE	CUSTOMER DESIGN CHANGE
21	V_{OUT}	21	V_{OUT}	DC / DC Boost Circuit Output External DC / DC Boost Input	Voltage polarity change.	None
		22	C4+		Voltage Polarity Signal Name Pin Numbering due to added boost cap connection.	None
22	C3-	23	C3+			
23	C1+	24	C1-			
24	C1-	25	C1+			

F-51851 PIN	F-51851 NAME	F-55471 PIN	F-55471 NAME	FUNCTION	F-51851 to F-55471 DESIGN CHANGE	CUSTOMER DESIGN CHANGE
25	C2-	26	C2+			
26	C2+	27	C2-			
27	V_1	28	V_1	Voltage Follower Output External Voltage Supply Input	Voltage polarity & magnitude change, Pin Number. F-51851 – 1/9 x (V_{DD}-V_5). F-55471 – 8/9 x (V_0-V_{SS})	Change external power supply circuit to match FIGURE 8. Connect to display per FIGURE 7 OPTION 3. Match pin numbering.
28	V_2	29	V_2		Voltage polarity & magnitude change, Pin Number. F-51851 – 2/9 x (V_{DD}-V_5). F-55471 – 7/9 x (V_0-V_{SS})	
29	V_3	30	V_3		Voltage polarity & magnitude change, Pin Number. F-51851 – 7/9 x (V_{DD}-V_5). F-55471 – 2/9 x (V_0-V_{SS})	
30	V_4	31	V_4		Voltage polarity & magnitude change, Pin Number. F-51851 – 8/9 x (V_{DD}-V_5). F-55471 – 1/9 x (V_0-V_{SS})	
31	V_5	32	V_0		Voltage polarity & magnitude change, Pin Number. LCD driving voltage magnitude (V_0-V_{SS}) is lower due to new liquid crystal. F-51851 – V_5 is large negative voltage. F-55471 – V_0 is large, positive voltage.	
32	VR	33	VR		Voltage polarity & magnitude change, Pin Number.	None
33	C86	34	C86	Select µP Interface (68- or 80-type)	Pin Number	Match Pin Number
34	P/S	35	P/S	Select Parallel / Serial Interface	Pin Number	Match Pin Number
35	NC	36	IRS	select internal / external gain resistors for voltage regulator.	Pin Number	Match Pin Number
36	NC					

11.0 SPECIFICATION ERRATA

The following sections provide corrections to the specifications.

11.1. The F-55472GNFQJ-LB-AEN LCD Module Specification refers to drawing F-55472 AB Base. Ths drawing shows 4 LEDs. The correct number of LEDs for a blue backlight display is seven.

END_OF_FILE