# THE IMPACT OF ENERGY EFFICIENCY STANDARDS ON STANDBY POWER IN CONSUMER ELECTRONICS DESIGN

A Lattice Semiconductor White Paper

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## *Regulatory Measures to Reduce Standby Power*

Squeezing every last microwatt from a system is a common objective for engineers who are designing battery operated equipment. And as more strict government regulations regarding power consumption appear, even traditional home and office appliances like LCD TVs, set top boxes (STBs) and multi-function printers (MFPs) are being scrutinized for ways to save power. To help ensure products are in compliance with the latest EnergyStar and European Commission Code of Conduct regulations, designers are seeking innovative ways to provide low-power modes of operation in a variety of product lines. This white paper examines design methods and practical advice for saving power using programmable logic devices (PLDs).

The 1-Watt Plan is an energy saving proposal by the International Energy Agency (www.iea.org) to reduce standby power use in all appliances to just one watt. Standby power, also called vampire or phantom power, refers to the electricity consumed by many appliances when they are switched off or in standby mode. The typical power loss per appliance is low (from 1 to 25 W), but when multiplied by the billions of appliances in residential and commercial use, standby losses represent a significant fraction of total world electricity use. Research indicates that standby power accounts for as much as 7-13% of household power consumption.

While the definition of standby power use depends on the product being analyzed, standby power includes at a minimum the power used while the product is performing no function. PLDs are increasingly being applied to maximize the amount of circuitry that can be unpowered or placed in a standby/sleep mode when the system is idle.

Since modern programmable logic devices (PLDs) have very low static current requirements, often in the microampere range, they are ideal as system event

monitors to control overall system wake/sleep states. An example of an ultra-low power PLD is the Lattice Semiconductor ispMACH 4000ZE Complex PLD (http://www.latticesemi.com/products/cpldspld/ispmach4000ze). The typical static current consumption for a 64-macrocell 4000ZE is 15 microamperes (μAs), which makes it an ideal "sentinel" for detecting events that require the overall system to be wakened from sleep or hibernate states.

## *PLDs as System Sleep Managers*

One of the technical solutions to the problem of reducing standby power is a smart electronic switch that cuts power when there is no load, or after some period of inactivity, and restores it immediately when required. PLDs are used with popular application chipsets to reduce standby power and minimize the time that key processors need to be powered on to detect system events. Power management is a feature of some electrical appliances, especially set top boxes (STB), computers and computer peripherals such as monitors and printers, that turns off the power or switches the system to a low-power state when inactive.

Wake-on-LAN (WoL) is an Ethernet computer networking standard that allows a computer to be turned on or awakened by a network message. The message is usually sent by a simple program executed on another computer on the local area network. Low cost IP-TV STBs and multi-function printers (MFPs) are ideal appliances to use Ethernet WoL as an interrupt to pull a power-hungry application processor out of sleep mode. A CPLD, with its low current requirement, is a good candidate for a smart switch to detect Ethernet traffic to a printer or STB.

Within a STB architecture, as program updates or subscription content is pushed from the headend to the customer, their arrival can "wake up" the idle STB when it is addressed. An always-on, low-power CPLD like the ispMACH 4000ZE can quickly respond when the device is addressed by the network but also keep

current consumption to a minimum. A fast CPLD is required to detect incoming frames because traditional low-cost, low-speed microcontrollers can not reliably detect incoming data on the media independent interface bus (MII) operating at 25 MHz. The 64-macrocell 4064ZE -4 speed grade device supports a minimum register setup time of 2.5 ns to support rapid decoding of IOs. A unique MAC address is programmed into the smart switch CPLD during an automated factory programming step.

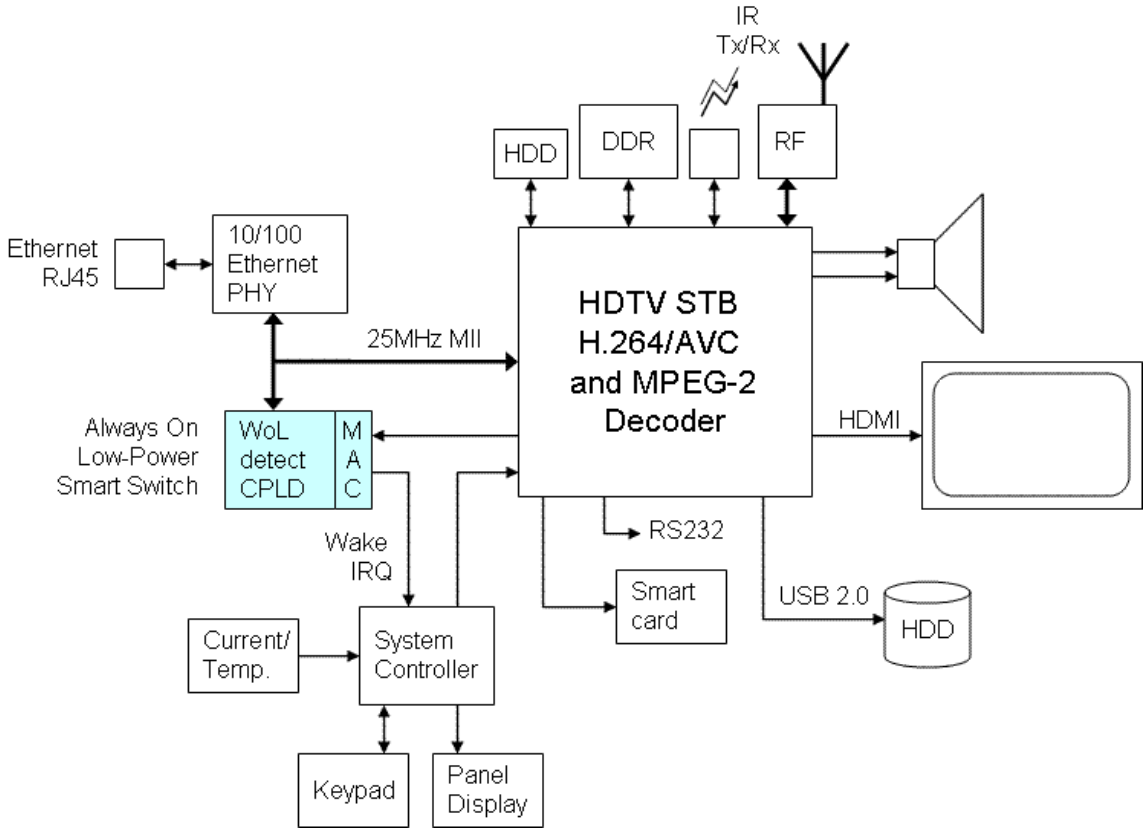


**Figure 1 - IP-TV STB with CPLD-based Smart Switch**

Another energy saving measure used in modern electronics is to selectively operate subsystems depending on demand by controlling when a subsystem clock is enabled. Reducing the periods the circuit is operating dynamically can reduce current consumption.

## *Clock Gating with PLDs*

Clock gating is one of the power saving techniques used on many synchronous circuits. To save power, clock gating support adds additional logic to a circuit to prune the clock tree, disabling portions of the circuitry so that its flip-flops do not change state: their switching power consumption goes to zero, and only leakage currents are incurred.

Clock gating instructs the hardware to detect whether there's any work to do, and to turn off a given clock if it isn't needed. For example, a bridge or bus might use automatic gating so that it's gated off until an application processor needs to use it, while several of the peripherals on that bus might be permanently gated off if they are unused on that board.

A PLD coupled with an inexpensive crystal Pierce RC circuit can provide an automatic hardware clock gating method. The Lattice Application Note AN8080 (http://www.latticesemi.com/documents/an8080.pdf) describes the method using an ispMACH 4000ZE or a MachXO PLD. The circuit in Figure 2 is an implementation for a gated real time clock (RTC) source at 32.768 kHz, a clock commonly found in handheld devices like smartphones.

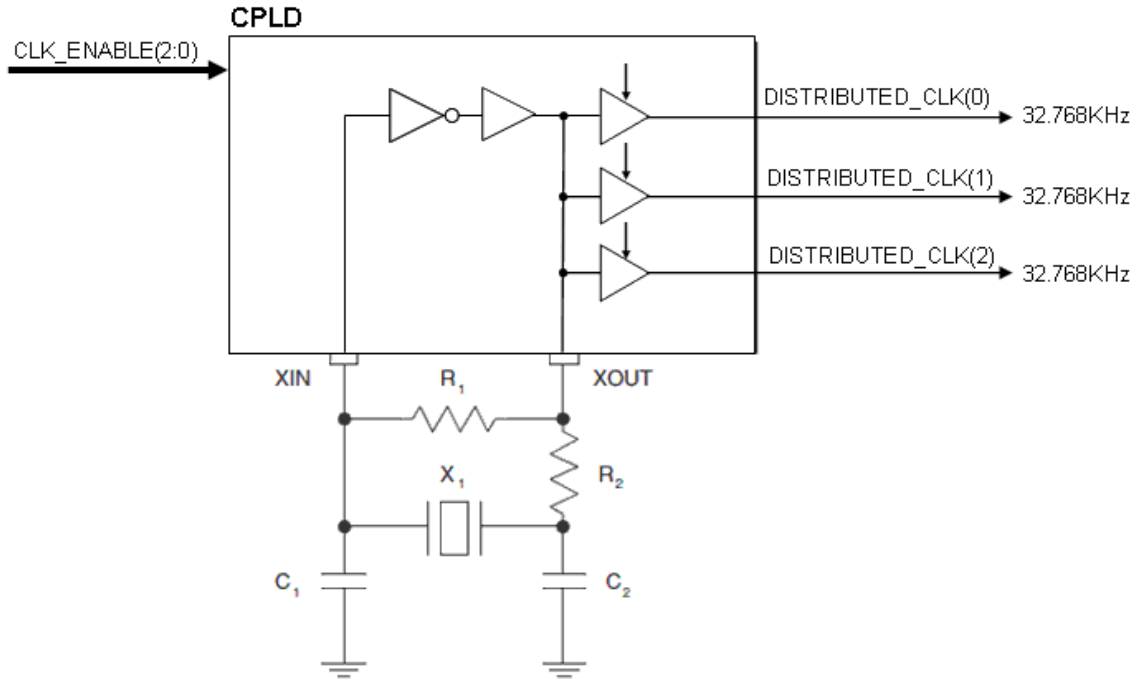


**Figure 2 - CPLD with Crystal Pierce Circuit**

Crystals are a low cost and accurate clocking alternative that can be used in a number of applications. Crystals are available in frequencies from 30 kHz to 50 MHz using the fundamental resonant frequency. A Pierce circuit is recommended for crystal implementation due to its simplicity, low cost and robustness. The designer will use the CL formulas and rules of thumb to specify the initial values for C1 and C2 in Figure 2 and use bench testing to finalize these values. The CLK_ENABLE (2:0) input enables the individual DISTRIBUTED_CLK (2:0) outputs to enable/disable subsystems to minimize power.

## *Power Saving Techniques for PCBs*

Current leakage paths on PCBs contribute to battery drain and phantom power, but some simple circuit techniques can help. For example, when Lattice developed its ispLEVER 4000ZE Pico Development Kit (http://www.latticesemi.com/products/developmenthardware/developmentkits/ispmach4000zepicodevkit.cfm), one of the quality criteria was that the board must

have very low static power consumption when not operating. The board would be used by engineers who would often store the board for extended periods with the 3V thumb battery installed. Current leakage paths had to be removed to avoid draining the battery. The Pico board uses a variation of the clock gating method, in this case enabling only certain power rails when required. In this scenario, sensor amplifiers were powered on only when the CPLD requested a measurement. Upon request, the CPLD asserts the ENABLE input, connecting the 3.1V battery support and energizing the sensor circuits. Once the data is retrieved by the CPLD, the enable is released and sensors are unpowered.

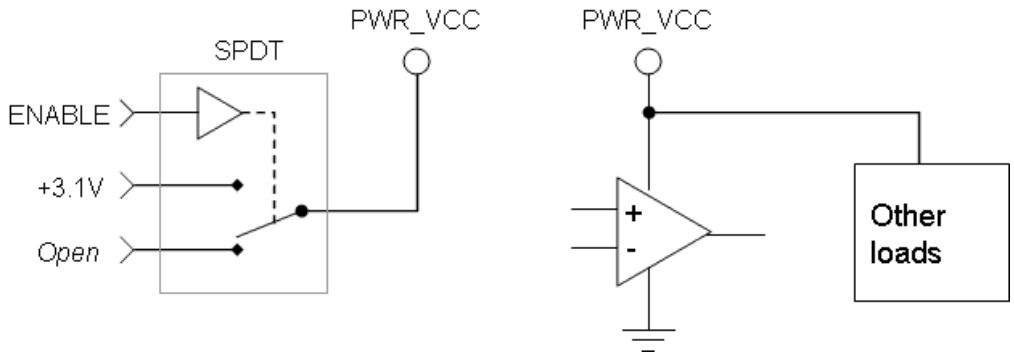


**Figure 3 - Gating of On-Board Power Rails**

## *Conclusion*

Low power PLDs have emerged in a variety of roles to serve as smart switches to “wake” idle chip sets and, when integrated with an inexpensive crystal, can serve to gate clock networks. PLDs have proven to be a valuable tool to help reduce system power consumption in electronic products. As more strict government power consumption regulations are applied, standby current consumption becomes an important consideration for designers.

## References

1. ACPI (http://en.wikipedia.org/wiki/Advanced_Configuration_and_Power_Interface)

2. EnergyStar (http://www.energystar.gov)

3. EU Standby Initiative
(http://re.jrc.ec.europa.eu/energyefficiency/html/standby_initiative.htm)

4. ispMACH 4000ZE CPLD
(http://www.latticesemi.com/products/cpldspld/ispmach4000ze/)

5. ispMACH 4000ZE Pico Development Kit
(http://www.latticesemi.com/products/developmenthardware/developmentkits/ispmach4000zepicodevkit.cfm)

6. One Watt Initiative (http://en.wikipedia.org/wiki/One_Watt_Initiative)

7. Power Estimation in ispMACH 4000ZE Devices, TN1187
(http://www.latticesemi.com/documents/tn1187.pdf)

8. Things that Go Blip in the Night – Standby Power and How to Limit It, International Energy Agency,
(http://www.iea.org/textbase/nppdf/free/2000/blipinthenight01.pdf)

9. Using a Discrete Crystal as a PLD Clock Source, Lattice Semiconductor Corporation, AN8080 (http://www.latticesemi.com/documents/an8080.pdf)