APPLICATION NOTE

Mapping Mono Data to Stereo Channel

Mono Audio Codec with Speaker Driver

1. DIGITAL AUDIO INTERFACES

WAU8812 is a Mono audio codec; supports standard audio interface which by definition has two separate channels Left and Right for data. In normal mode, WAU8812 receives Mono data through the analog inputs and output digital data through the ADCOUT pin. Since WAU8812 is a Mono device, it only output Left channel data. Although WAU8812 is a Mono device, it includes a L/R Fill mode where Left channel data is copied to the Right channel. This feature is enabled by setting LRDAT[2] address (0x3C) to "1". In L/R Fill mode, the Mono audio data is simultaneously in both the Right and Left channel. It is NOT a real stereo mode. The resultant of this feature is stereo like sound. This feature is implemented on to all the audio interfaces supported by WAU8812. The default audio format is I^2S interface.

1.1. Right Justified audio data

In right justified interface (normal mode), the left channel serial audio data is synchronized with the frame sync. Left channel data is transferred during the HIGH frame sync. The MSB data is sampled first. The data is latched on the last rising edge of BCLK before frame sync transition (FS). The LSB is aligned with the falling edge of the frame sync signal (FS). Right justified format is selected by setting AIFMT[1:0] address (0x04) to "00" binary in conjunction with PCMTSEN[8] address (0x3C) set to LOW.

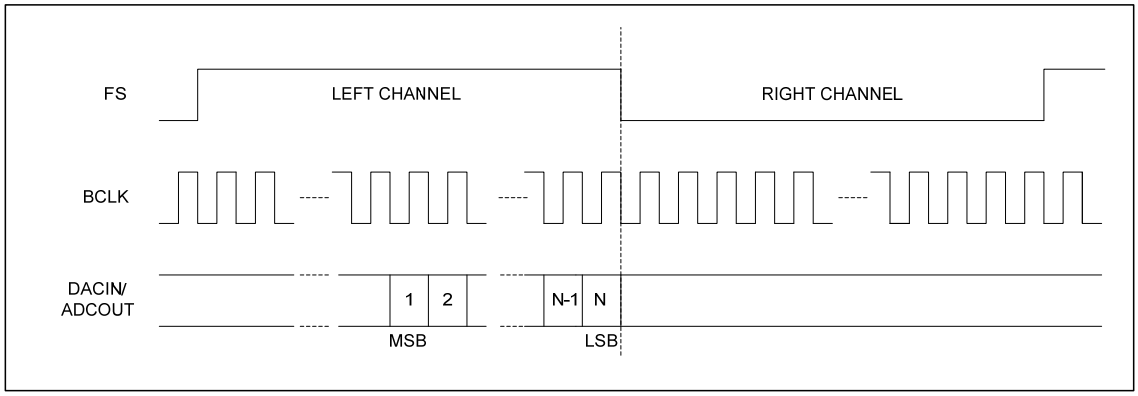

Figure 1: Right Justified Audio Interface (Normal Mode)

WAU8812 features a L/R Fill mode where the device outputs Left channel data to both Left and Right channels. This is accomplished by setting LRDAT[2] address (0x3C) to "1".

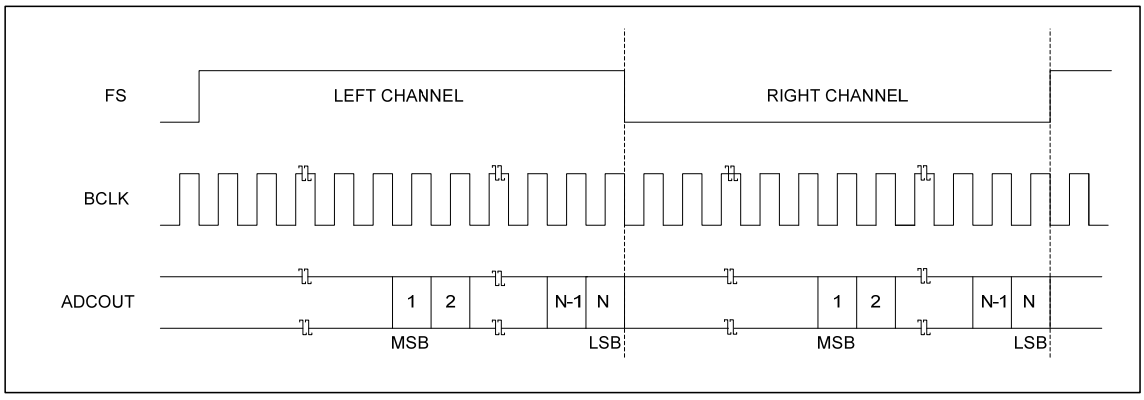

Figure 2: Right Justified Audio Interface (L/R Fill mode)

1.2. Left Justified audio data

In Left justified interface (normal mode), the left channel serial audio data is synchronized with the frame sync. Left channel data is transferred during the HIGH frame sync. The MSB data is sampled first. The data is latched on the first rising edge of BCLK following a frame sync transition (FS). Left justified format is selected by setting AIFMT[1:0] address (0x04) to "01" binary in conjunction with PCMTSEN[8] address (0x3C) set to LOW.

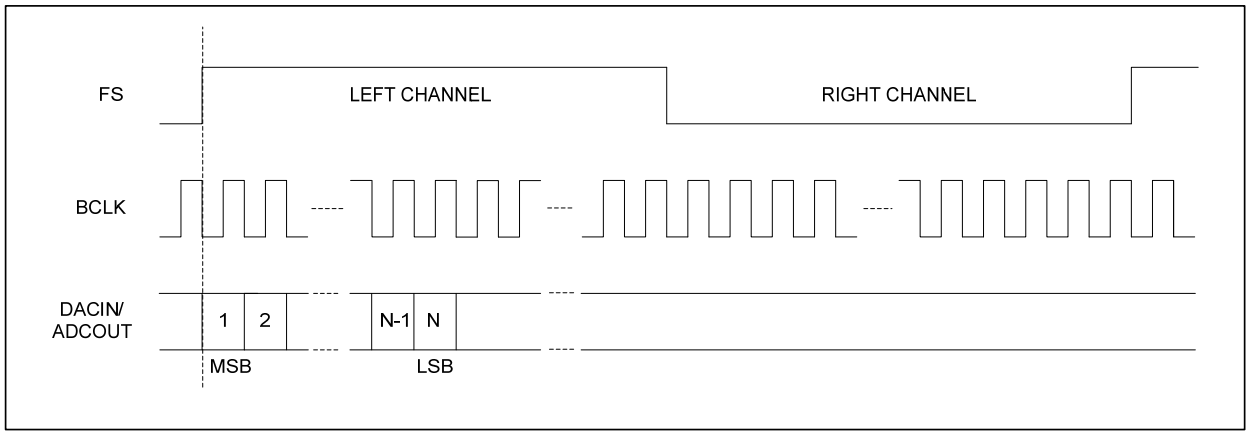

Figure 3: Left Justified Audio Interface (Normal Mode)

WAU8812 features a L/R Fill mode where the device outputs Left channel data to both Left and Right channels. This is accomplished by setting LRDAT[2] address (0x3C) to "1".

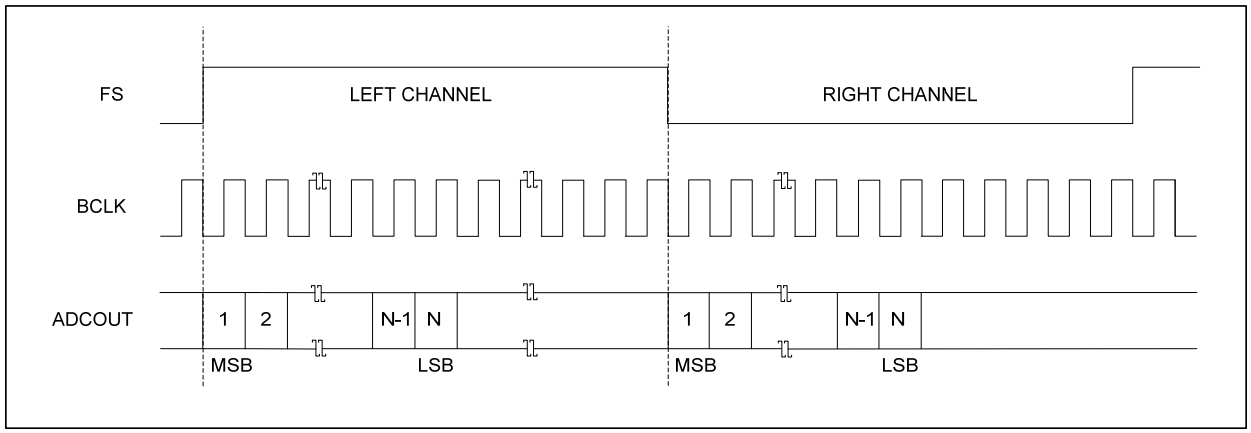

Figure 4: Left Justified Audio Interface (L/R Fill mode)

1.3. I²S audio data

In I²S interface (normal mode), the left channel serial audio data is synchronized with the frame sync. Left channel data is transferred during the LOW frame sync. The MSB data is sampled first. The data is latched on the second rising edge of BCLK following a frame sync transition (FS). I²S format is selected by setting AIFMT[1:0] address (0x04) to "10" binary in conjunction with PCMTSEN[8] address (0x3C) set to LOW.

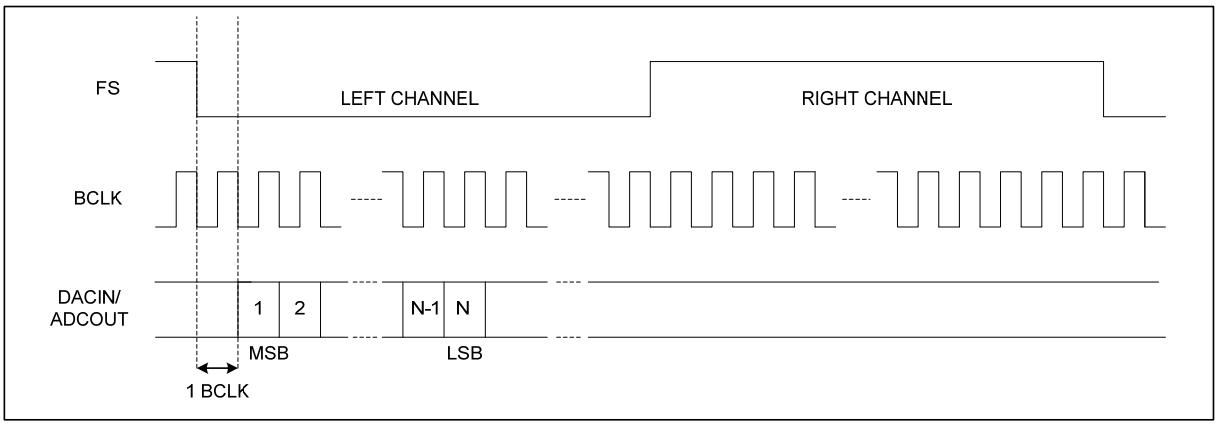

Figure 5: I2S Audio Interface (Normal Mode)

WAU8812 features a L/R Fill mode where the device outputs Left channel data to both Left and Right channels. This is accomplished by setting LRDAT[2] address (0x3C) to "1".

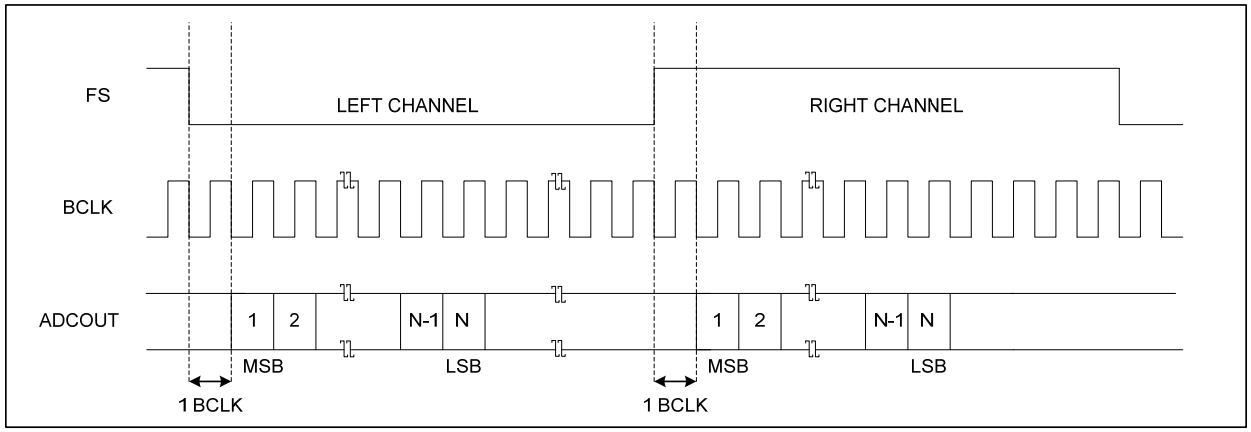

Figure 6: I2S Audio Interface (L/R Fill mode)

1.4. PCM audio data

In PCM interface (normal mode), the left channel serial audio data is synchronized with the frame sync. Left channel data is transferred during the LOW frame sync. The MSB data is sampled first. The data is latched on the second rising edge of BCLK following a frame sync transition (FS). PCM format is selected by setting AIFMT[4:3] address (0x04) to "11" binary in conjunction with PCMTSEN[8] address (0x3C) set to LOW.

The digital data can be forced to appear on the right phase of the FS by setting ADCPHS[0] and DACPHS[1] address (0x04) bits to HIGH respectively. The starting point of the right phase data depends on the word length WLEN[6:5] address (0x04) after the frame sync transition (FS).

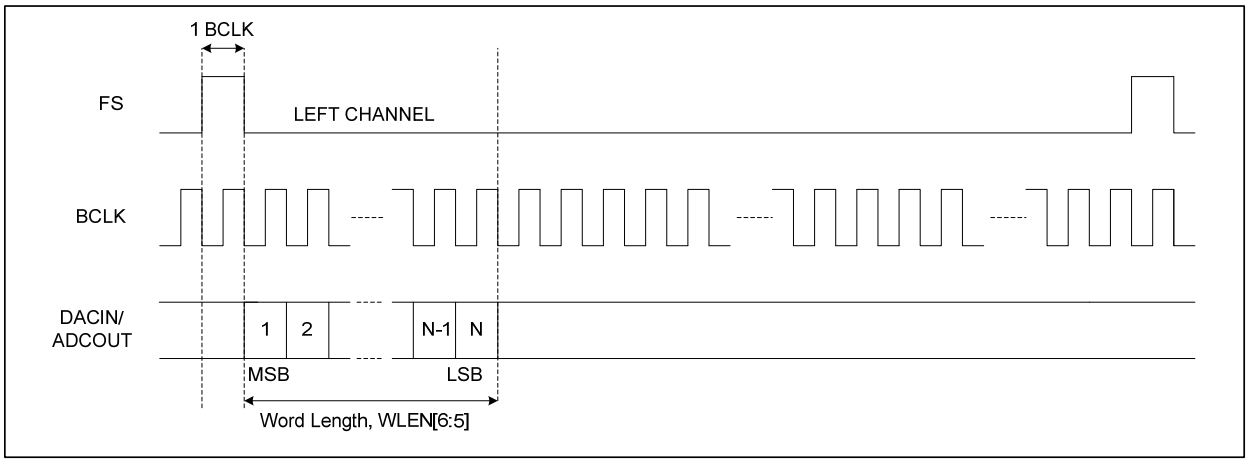

Figure 7: PCM Mode Audio Interface (Normal Mode)

WAU8812 features a L/R Fill mode where the device outputs Left channel data to both Left and Right channels. This is accomplished by setting LRDAT[2] address (0x3C) to "1".

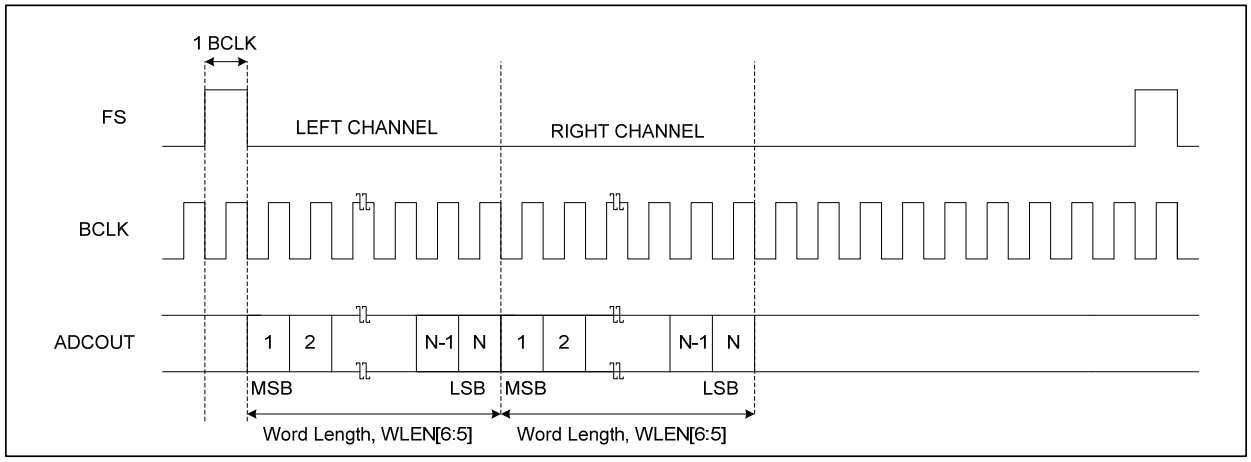

Figure 8: PCM Mode Audio Interface (L/R Fill mode)

1.5. PCM Time Slot audio data

In PCM Time-Slot interface (normal mode), the left channel serial audio data is synchronized with the frame sync. Left channel data is transferred during the LOW frame sync. The MSB data is sampled first. The starting point of the timeslot is controlled by a 10-bit byte TSLOT[9:0] address (0x3B and 0x3C). The data is latched on the first rising edge of BCLK following a frame sync transition (FS) providing PCM is in timeslot zero (TSLOT[9:0] = 000). PCM Time-Slot format is selected by setting AIFMT[4:3] address (0x04) to "11" binary in conjunction with PCMTSEN[8] address (0x3C) set to HIGH.

The digital data can be forced to appear on the right phase of the FS by setting ADCPHS[0] and DACPHS[1] address (0x04) bits to HIGH respectively. The starting point of the right phase data depends on the word length WLEN[6:5] address (0x04) and timeslot assignment TSLOT[9:0] address (0x3B and 0x3C) after the frame sync transition (FS).

DACIN will return to the bus condition either on the negative edge of BCLK during the LSB, or on the positive edge of BCLK following the LSB depending on the setting of TRI[7] address (0x3C). Tri-stating on the negative edge allows the transmission of data by multiple sources in adjacent timeslots without the risk of driver contention.

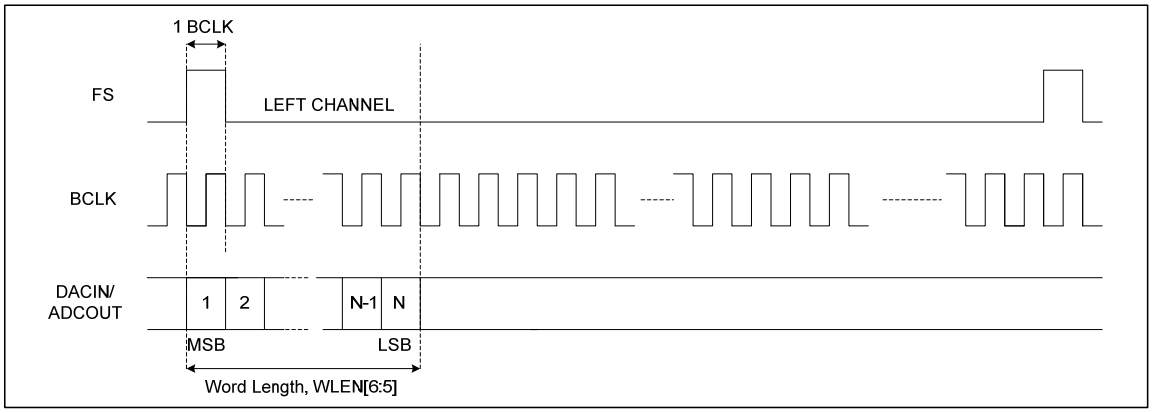

Figure 9: PCM Time Slot Mode (Time slot = 0) (Normal Mode)

WAU8812 features a L/R Fill mode where the device outputs Left channel data to both Left and Right channels. This is accomplished by setting LRDAT[2] address (0x3C) to "1".

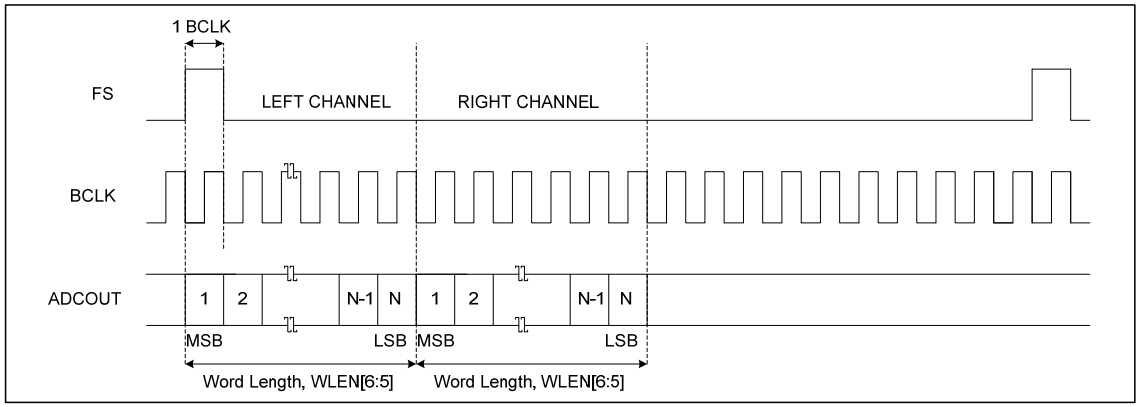

Figure 10: PCM Time Slot Mode (Time slot = 0) (L/R Fill mode)

2. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1.0	May 2009		