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# Quasi-clamped Inductive Switching Behaviour of Power Mosfets

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***Abstract* - Turn off behaviour of power Mosfets with Quasi-clamped Inductive Switching (QIS) loads is analysed. In most real applications the main inductive load is clamped during turn off but there is enough unclamped inductance in the circuit to cause voltage spikes and avalanche breakdown. This is the QIS situation and occurs in almost all practical circuits from motor drives to inverters to VRMs. Analytical expressions are derived for turn off losses under QIS which take into account the unclamped inductance in the circuit, gate drive parameters and more importantly, the source inductance of the package. The equations also predict the peak voltage during turn off and the conditions that would drive the device into avalanche.**

**A common solution for avalanche prevention during inductive turn off is the protected Mosfet with an integrated drain to gate zener diode. The zener diode forces the Mosfet to turn on, thereby clamping the drain voltage. The trade offs in the design of such protected Mosfets are analysed. The findings are verified in the practical case of a power tool where the motor speed is controlled by PWM operation of a single switch. The circuit has large unclamped inductances arising from wiring and very high peak currents under locked rotor conditions. It is shown that a well designed Mosfet with avalanche protection can survive the locked rotor condition for longer durations, thereby increasing the overall product reliability.**

## INTRODUCTION

The inductive turn off of power devices has been analysed in detail, [1] – [6]. However the literature has concentrated on two extremes; one is the totally unclamped inductive switching, as in automotive applications where the device is allowed to go into avalanche with the specified load current by default, and survive. The other case, known simply as "inductive turn off" refers to the situation where the peak switch voltage is predictably clamped, either by topology as in a synchronous buck or an inverter, or by a snubber as in a flyback converter. By default there is no other unclamped inductance in the circuit. Fig 1) shows the conventional turn off waveforms.

The corresponding time intervals are

$T_0$ – Gate voltage fall time from $V_{gs}$ to $V_{gp}$. No change occurs in $V_{ds}$ or $I_{ds}$

$T_{v\_rise}$ – Plateau time at $V_{gp}$. Vds rises from a low saturated level to $V_{in}$. $I_{ds}$ does not change

$T_{i\_fall}$ – Current falls from peak $I_{ds}$ to 0A as $V_{gs}$ falls from plateau voltage $V_{gp}$ to gate threshold $V_{th}$

$T_3$ – $V_{gs}$ falls from $V_{th}$ to zero. Turn off is complete.

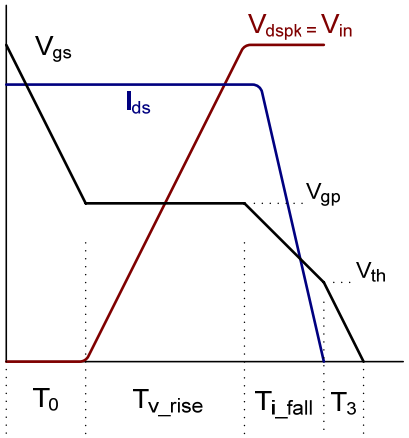


Fig 1) Inductive turn off waveforms.

The reality is quite at variance with the simple model above. Practical measurements show that the current fall times are much longer than what the gate drive conditions predict. Given that there will always be some parasitic inductance in the circuit that lies outside the clamp, the peak voltage seen by the switch will be higher than $V_{in}$ and complicated further by the resonant ringing of the circuit inductance with the output capacitance of the switch. A more practical analysis is needed taking into account parasitic inductances both in the circuit and the package to predict the turn off behaviour. The source inductance, in combination with total circuit inductance, influences not only the switching behaviour and the losses, but also the peak turn off voltage and avalanche breakdown. Fig 2) shows the Quasi-clamped Inductive Switching (QIS) circuit used in this analysis. $L_{ckt}$ represents the parasitic circuit inductance that lies outside the freewheeling diode. Fig 3) shows the turn off waveforms with corresponding time intervals.

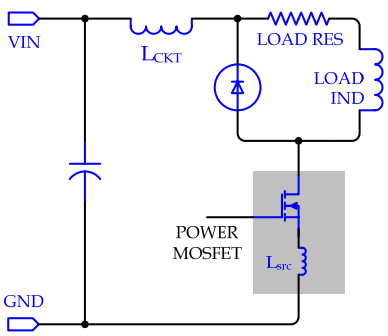


Fig 2) Quasi-clamped Inductive Circuit

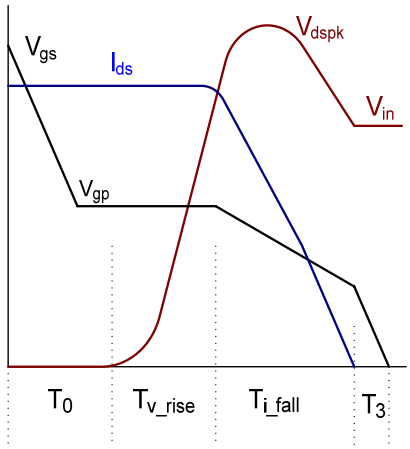


Fig 3) Switching waveforms for QIS

## SWITCHING TIME CALCULATIONS DURING TURN OFF

Usually the voltage rise time is written in terms of the gate to drain Miller charge $Q_{gd}$. However it is found that $Q_{gd}$ is not a reliable parameter to predict the voltage rise time. Fig 4) shows the simulation of a Mosfet turn off under normal gate drive conditions. During inductive turn off with large gate currents, bulk of the drain to source voltage $V_{ds}$ transition is completed while the gate voltage is still at the Miller plateau. The standard test circuit for measuring $Q_{gd}$ uses a much smaller gate current and does not provide a practically usable parameter. The alternative is to use reverse capacitance $C_{rss}$, which unfortunately varies considerably with $V_{ds}$. Empirical measurements have shown that a value of 2 x $C_{rss}$ gives a better approximation of the rise time.

$$T_{v\_rise} = 2 \times C_{rss} \times V_{dspk} \times [(R_g + R_{snk})/ (V_{gs} - V_{gp}]$$

$R_{snk}$ is the equivalent series resistance of the gate drive circuit and $R_g$ is the internal gate resistance. $V_{dspk}$ is the peak drain to source voltage reached during the inductive turn off conditions and is an unknown at this stage. The term in square brackets is the inverse of gate turn off current and may be considered to be constant during the interval.

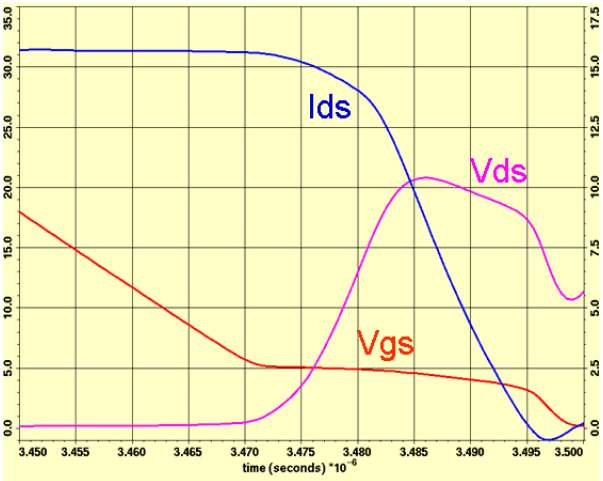


Fig 4) Turn off waveform simulations

Conventionally the current fall time is estimated as the time required by the gate to discharge from $V_{gp}$ to $V_{th}$, [3] and written as

$$T_{i\_fall} = C_{iss} \times (R_g + R_{snk}) \times \ln (V_{gp} / V_{th})$$

In reality the measured current fall times are much longer. The anomaly is readily explained if it is realised that there are three possible expressions for calculating the current fall time.

- Gate turn off time expressed by

  $C_{iss} \times (R_g + R_{snk}) \times \ln (V_{gp} / V_{th})$
- di/dt of the circuit inductance, expressed by

  $(V_{dspk} - V_{in}) / L_{ckt}$

  $L_{ckt}$ is the total parasitic inductance in the circuit and can be estimated using the method in [7].
- Modified gate turn off time with package source inductance $L_{src}$ taken into account

The idealised "inductive switching" analysis assumes no parasitic inductances and clamps $V_{dspk}$ to $V_{in}$. This is of little practical value. Without this assumption we can write a generic expression for $V_{dspk}$ as

$$V_{dspk} = V_{in} + L_{ckt} \times di/dt \qquad (1)$$

A simplifying assumption made in this analysis is that the current falls linearly from $I_{ds}$ to zero i.e. $V_{dspk}$ is constant during the current fall. If the fall time is dominated entirely by parasitic inductances,

$$di_{ds} / dt = I_{ds} / T_{i\_fall}$$
$$= (V_{dspk} - V_{in}) / L_{ckt} = V_{src} / L_{src}. \qquad (2)$$

The critical parameter now is $V_{src}$, the voltage across source inductance within the package, and given by $L_{src} \times di_{ds} / dt$. Realising that di/dt is same for source as well as circuit inductances is the key to solving for $V_{dspk}$. The presence of source inductance and its voltage $V_{src}$ extends the gate transition time from $V_{gp}$ to $V_{th}$, which is also the current fall time. The modified expression for gate turn off and $T_{i\_fall}$ is,

$$T_{i\_fall} = C_{iss} \times (R_g + R_{snk})$$
$$\times \ln [(V_{gp} - V_{src}) / (V_{th} - V_{src})] \qquad (3)$$

Eliminating $T_{i\_fall}$ from (2) and (3) gives us two expressions for $V_{dspk}$ and $V_{src}$

$$V_{dspk} = V_{in} + ( L_{ckt} / L_{src} ) * V_{src} \qquad (4)$$

This is the circuit inductance based solution. The next expression can be described as the gate drive based solution and written as

$$V_{dspk} = V_{in} + \frac{L_{ckt} \times I_{out}}{C_{iss} \times (R_g + R_{snk}) \times \ln [(V_{gp} - V_{src}) / (V_{th} - V_{src})]} \qquad (5)$$

Despite the logarithmic term in the denominator, equations (4) and (5) can be solved for $V_{src}$ and $V_{dspk}$, using simple numerical methods. Note that $V_{dspk}$ has an upper limit at the avalanche breakdown voltage $BV_{ds}$, typically 1.3 times the $V_{ds}$ rating of the device. The source voltage $V_{src}$ also has an upper limit at the gate

threshold $V_{th}$. We can evaluate equations (4) and (5) for a range of assumed $V_{src}$ values from 0 to $V_{th}$. The solution is that value of $V_{src}$ where equation (4) and (5) yield the same result for $V_{dspk}$. In other words the *peak turn off voltage as well as current fall time should be same whether they are calculated using circuit inductances or by gate turn off expressions*. Once $V_{dspk}$ is found, $T_{i\_fall}$ can be estimated from equation (3) and the turn off loss can be written as

$$P_{swoff} = \tfrac{1}{2} V_{dspk} \times I_{out} \times ( T_{v\_rise} + T_{i\_fall} ) \times F_{sw} \qquad (6)$$

The effect of source inductance has been covered in several application notes and papers, [8]–[11]. It is generally agreed that larger source inductance causes less $V_{dspk}$, reduced ringing and shoot through, but at the same time increases the turn off switching loss. Equations (3) to (6) above explain why it is so.

## EXPERIMENTAL VERIFICATION

As an example the turn off behaviour of a power device AOT430 in TO-220 package was studied in a power tool application. This device has a $C_{iss}$ = 4.7 nF, effective $V_{th}$ = 3.0V and $V_{ds}$ rating of 75V with an expected avalanche breakdown just below 100V. The typical drain to source $R_{ds}$ value is 11 mΩ. During the tests input voltage, switching current and frequency and duty ratio were set to 24V, 10 kHz and 70% respectively. These were intended to duplicate the combination of worst case stresses such as the locked rotor condition, seen in the power tool. On the bench set up turn off waveforms were captured over a range of circuit inductances and peak currents and compared with predicted values.

A source inductance value of 12.5 nH was used in the calculations, of which 7.5 nH comes from within the TO-220 package and the rest from mounting with uncut leads. Gate turn off current was measured during $T_{i\_fall}$ and a gate series resistance of 10Ω was estimated. A spreadsheet was written to calculate the $V_{dspk}$ during turn off as a function of drop across the source inductance using both gate drive conditions and di / dt in the circuit inductance. The operating point is where the two curves intersect, within the limits imposed by $V_{th}$ and $BV_{ds}$. Depending on operating conditions two other solutions are possible. If the curves do not intersect even at $V_{src}$ = $V_{th}$, the current fall is dominated by the parasitic inductance and gate drive has very little influence on it. At the other extreme, with large circuit inductances and/or fast gate drives the device will go into avalanche, indicated by a region where both curves will share a common value of $BV_{ds}$.

Figs 4a) and b) show calculated and measured results for a circuit inductance of 150 nH. The turn off is dominated by circuit inductance which clamps the $V_{src}$ at its maximum of 3V. If the current is reduced to 50A, the two curves do intersect and the results are shown in Figs 5a) and 5b). Note that the $V_{gs}$ waveform includes the source inductance voltage inside the package, which is almost equal to $V_{th}$ because of the large parasitic inductances that were introduced in the circuit.

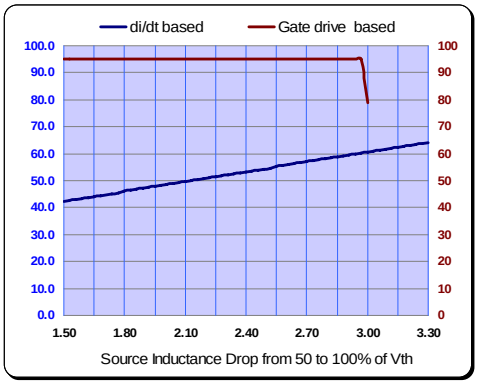


Fig 4a) Calculation of $V_{dspk}$ with $L_{ckt}$ = 150 nH and $I_{ds}$ = 100A

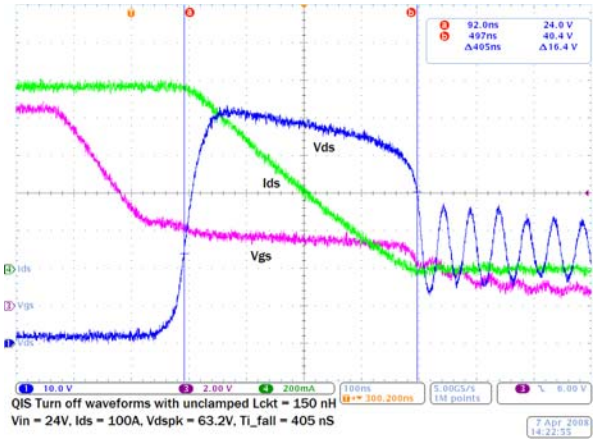


Fig 4b) QIS Turn off waveforms with $L_{ckt}$ = 150 nH and Ids = 100A

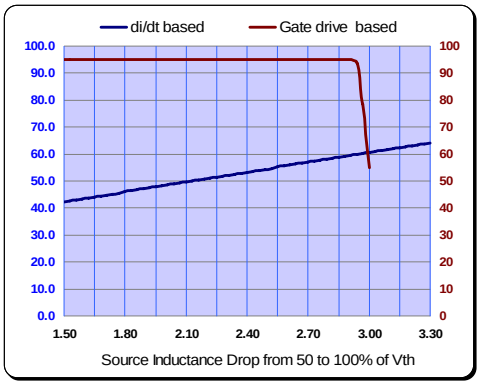


Fig 5a) Calculation of $V_{dspk}$ with $L_{ckt}$ = 150 nH and $I_{ds}$ = 50A

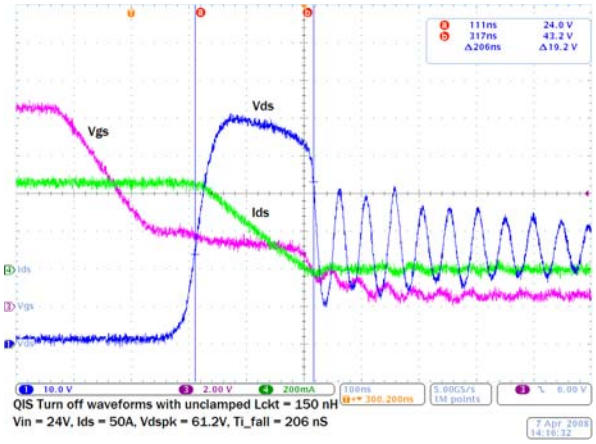


Fig 5b) QIS Turn off waveforms with $L_{ckt}$ = 150 nH and Ids = 50A

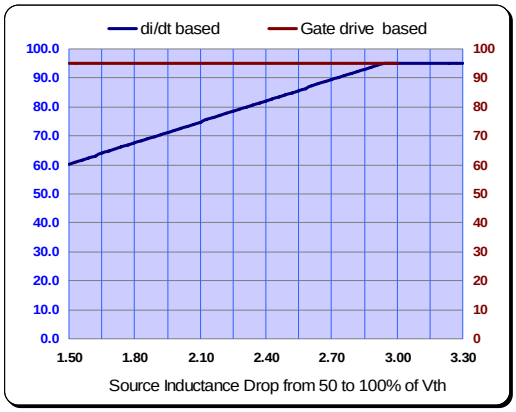


Fig 6a) Calculation of $V_{dspk}$ with $L_{ckt}$ = 300 nH and $I_{ds}$ = 100A

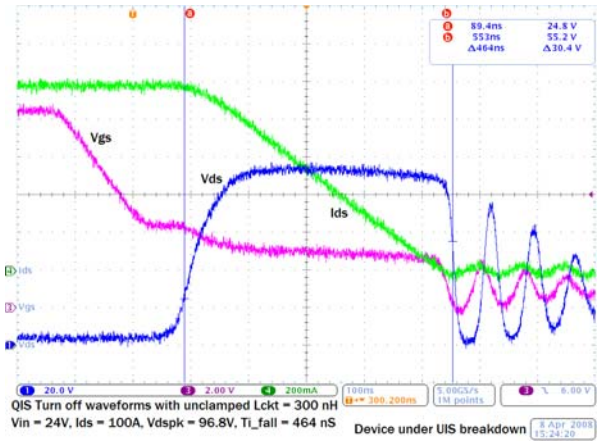


Fig 6b) QIS Turn off waveforms with $L_{ckt}$ = 300 nH and $I_{ds}$ = 100A.

Figs. 6a) and 6b) above show the results for circuit inductance of 300 nH. Avalanche breakdown is predicted, as seen by the upper $BV_{ds}$ limit in Fig 6a), and observed in Fig. 6b). A simple variation can be tried to demonstrate the role source inductance plays in determining the peak $V_{ds}$ and the avalanche condition. With 300 nH inductance still in place, a very short wire was added to source lead increasing $L_{src}$ by no more than 2-3 nH. Calculations predict that the peak voltage should drop by about 10V, avoiding the avalanche breakdown but current fall time will increase as a result. Fig 7) shows the actual waveforms that confirm the analysis.

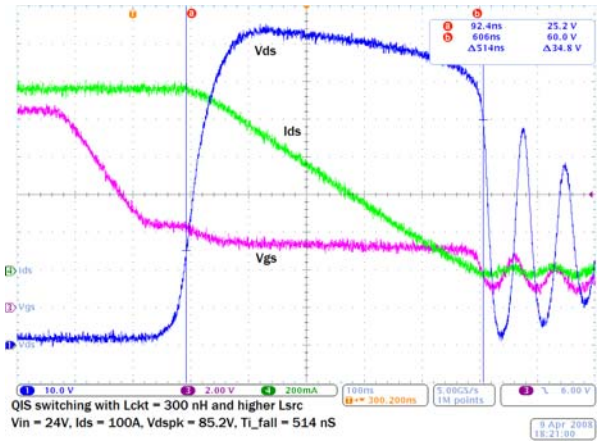


Fig 7) QIS Turn off waveforms with $L_{ckt}$ = 300 nH and $I_{ds}$ = 100A. Avalanche avoided by increasing $L_{src}$ to 15 nH.

TABLE I: PEAK $V_{ds}$ AND CURRENT FALL TIME CALCULATIONS

| Vds Condition | Lckt | Iout | Vdspk | | Tifall | |
|---|---|---|---|---|---|---|
| | | | Calc | Meas | Calc | Meas |
| | nH | Amp | Volts | | nS | |
| Unclamped | 70.0 | 100 | 41.2 | **43.4** | 348 | **371** |
| | | 50 | 41.2 | **42** | 174 | **185** |
| Unclamped | 150.0 | 100 | 60.2 | **63.2** | 386.4 | **405** |
| | | 50 | 60.2 | **61.2** | 193.2 | **206** |
| Unclamped | 250.0 | 100 | 84 | **85.6** | 400 | **438** |
| | | 50 | 84 | **82.4** | 200 | **232** |
| Avalanche | 300.0 | 100 | 95.9 | **96.8** | 403.5 | **464** |
| | | 50 | 95.9 | **95.2** | 201.7 | **247** |
| Lsrc added to avoid avalanche | 300.0 | 100 | 84.4 | **85.2** | 480 | **514** |
| | | 50 | 84.4 | **83.2** | 240 | **274** |

Table I above lists the calculated and measured values over the full range of circuit inductances and peak currents. The correlation between calculation and measured data improves with higher values of $L_{ckt}$ and $V_{dspk}$. The reason is that calculations assume a constant $V_{dspk}$ and predict its average value. As $V_{dspk}$ approaches $BV_{ds}$ it gets flatter, justifying the assumption.

So long as $V_{ds}$ is not clamped, the current fall time does not change much and di/dt rate remains within 10% of the calculated value of 260 A/uS. If $T_{i\_fall}$ were calculated using the standard gate drive based equations, without accounting for source inductance, the predicted fall time would be 5.1 nS.

## VOLTAGE CLAMPING

A common solution to the problem of excessive ringing and avalanche breakdown is to clamp the $V_{ds}$. If the clamp voltage is below the Mosfet breakdown limit, the device will not go into avalanche mode under any condition. However any attempt to clamp the peak voltage will invariably result in higher switching losses due to extended current fall times. Lower clamp voltages will result in successively longer turn off times and losses. Fig 8) shows an extreme case where the $V_{dspk}$ is clamped close to the supply voltage

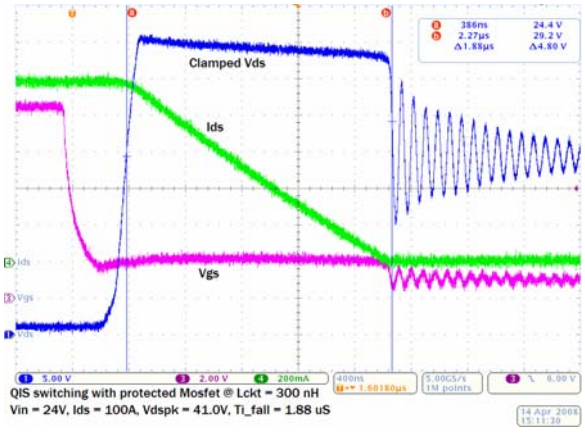


Fig 8) QIS Turn off waveforms with $L_{ckt}$ = 300 nH and $V_{ds}$ clamping close to supply voltage.

TABLE II: EFFECT OF $V_{ds}$ CLAMPING ON CURRENT FALL TIME

| Condition | Iout | Vdspk | Tifall |
|---|---|---|---|
| | Amp | Volts | nS |
| | | | |
| Vds under avalanche | 100 | 96.8 | 464 |
| | 50 | 95.2 | 247 |
| | | | |
| Vds clamped to 60V | 100 | 59.6 | 895 |
| | 50 | 59.6 | 450 |
| | | | |
| Vds clamped to 40V | 100 | 41 | 1880 |
| | 50 | 40.6 | 924 |
| | | | |
| **Lckt = 300 nH, Ids = 100A peak** | | | |

Table II above shows the effects of clamp voltage vs. $T_{i\_fall}$. The contribution to turn off losses from current fall time in equation (6) is $\frac{1}{2} V_{dspk} \times I_{out} \times T_{i\_fall} \times F_{sw}$.

This can be written as

$$P_{swi\_fall} = \frac{1}{2} L_{ckt} \times I_{out}^2 \times [\, 1 + V_{in} / (V_{dspk} - V_{in})] \qquad (7)$$

The switching losses are at their lowest as long as the drain voltage is allowed to reach the natural peak demanded by the circuit, and increase inversely as the drain voltage is clamped closer to $V_{in}$. Notice that in Fig 7) with the device forced to operate below avalanche the current fall time has increased to over 500 nS. Clamping the peak voltage lower and closer to $V_{in}$ will make the current fall time and losses much worse.

Despite the additional loss, there are applications where clamping the Mosfet may be the best option to avoid the avalanche breakdown and the associated latch up failures. One example is the PWM chopper for motor control used in a power tool. The basic block diagram is shown in Fig 9). The controller is a simple open loop circuit, implemented with logic gates or a timer like 555. The brake is a mechanical switch turned on to short the motor winding when the speed is set too low or turned off altogether. If the trigger speed is set >70%, the Mosfet is bypassed and battery is connected directly across the motor. Because of constructional constraints, the battery is located a few centimeters away from the Mosfet and the wiring can result in unclamped parasitic inductances as high as 500 nH. When the rotor is locked, large peak currents flow through the motor and the device, causing overshoots and/or avalanche breakdown.

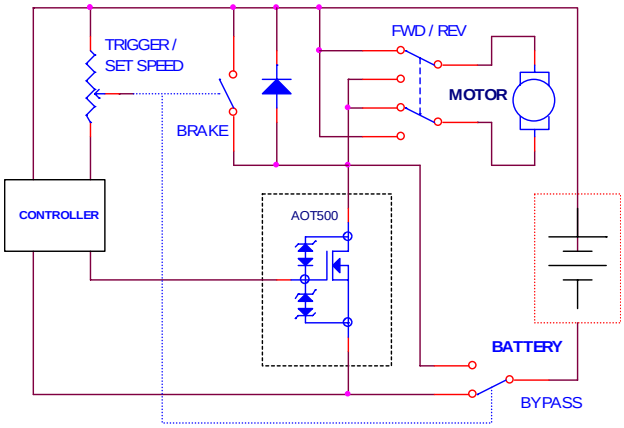


Fig 9) Electrical block diagram of a power tool

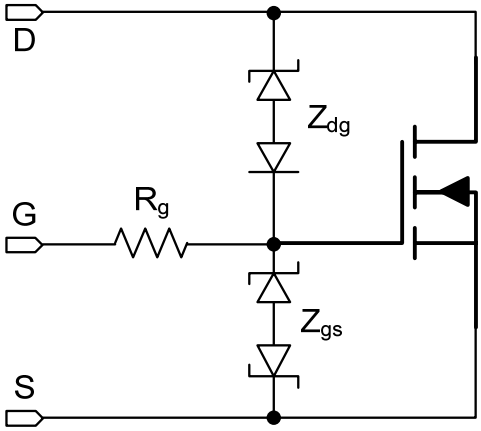


Fig 10) Graphical representation of protected Mosfet.

## PROTECTED MOSFETS

It is clear that the optimum design of Mosfet for such applications will require several trade offs, not the least of which is the overall cost. One such solution is a protected Mosfet. There are different levels of protections that can be bundled with a standard Mosfet package, such as overload, overtemperature and overvoltage. But for this application it was decided to put only a peak voltage clamp as shown in Fig 10). During turn off the $V_{dspk}$ will now be clamped to the zener voltage $V_{zdg} + V_{th}$, which obviously will be lower than $BV_{ds}$. The gate resistance is chosen to ensure that turn on threshold is reached even with gate pin grounded. The aim is to activate the device and allow it to absorb the parasitic energy through the channel. Power handling capability during inductive turn off will now come not from UIS rating but forward biased SOA which is much higher.

The next trade off is to determine the actual voltage ratings for the zeners as well the Mosfet. For a given die size and cost, reducing the voltage rating can exponentially cut down the $R_{ds}$ and the reduction in conduction loss can make up for the increased switching losses. Another benefit is that the normal operating efficiency will also improve due to lower $R_{ds}$, extending the battery life. With these considerations, various design choices were evaluated and the clamp was chosen at 40V for the protected Mosfet AOT500. Compared to the 75V 11 mΩ device, the protected version with the same die size has only half the $R_{ds}$ value. The turn off waveforms shown in Fig 8) came from this protected Mosfet.

Since the ability to survive the locked rotor condition for extended durations is the single most important benchmark of Mosfet performance in a power tool, the new protected device was compared with several others in that respect. Each Mosfet was attached to a small heatsink and allowed to switch high peak currents in the range of 60A to 80A continuously at 10 kHz with 18V and 24V input till they failed. The time to fail as well as the junction temperature were measured using a thermal camera. The results are shown in Table III. It is seen that the clamped Mosfet, despite the increased switching losses is more reliable, in that it lasts longer under extreme conditions.

TABLE III: PERFORMANCE OF THE PROTECTED MOSFET UNDER HIGH CURRENT CONDITIONS

| Ids | DUT | Vdspk | Duration | Tj | Result |
|---|---|---|---|---|---|
| | | | | | |
| 60A | AOT430 | 92V | 9 S | 230 $^{o}$C | Fail |
| 60A | AOT500 | 40V | 22 S | 213 $^{o}$C | Pass |
| 75A | AOT500 | 40V | 7 S | 240 $^{o}$C | Fail |

In addition to bench testing, the protected Mosfet was installed in a commercial power tool with an 18V, 1.7 AH battery pack. Two Mosfets were operated in parallel, and the locked rotor condition was maintained till the battery was fully discharged and the motor was shut off. For safety reasons it is specified that the power tool remain operational for at least 20 seconds under locked rotor conditions. The results show the requirement being met with adequate margin.

TABLE IV: PERFORMANCE OF THE PROTECTED MOSFET IN AN ACTUAL POWER TOOL

| Vdspk | Ids | Freq | Duty | Time |
|---|---|---|---|---|
| Volts | Amps | kHz | % | Seconds |
| | | | | |
| 39.4 | 88 | 7.4 | 65.9 | 35.2 |
| 39.2 | 93 | 6 | 69.7 | 34.8 |
| 39.4 | 92 | 6.6 | 69.6 | 35.7 |
| 39.2 | 91 | 7.2 | 65.7 | 35.9 |
| Note: Ids is the initial value of the peak current, which reduces over time as the battery discharges | | | | |

## ACKNOWLEDGEMENTS

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