

Nuvoton W681360 Linear CODEC Details

The Nuvoton W681360 Linear CODEC is slightly different from the familiar telephony CODECs. It does not do A-Law or μ -Law companding of the analog signals. It is converting the analog input to 13-bit PCM code words instead of the familiar 8-bit ones of the telephony CODECs. This 13-bit word is in 2's-Complement format. However, it has a special Sign-Extended Mode. There is also has a digital method of controlling the receive level of the analog output.

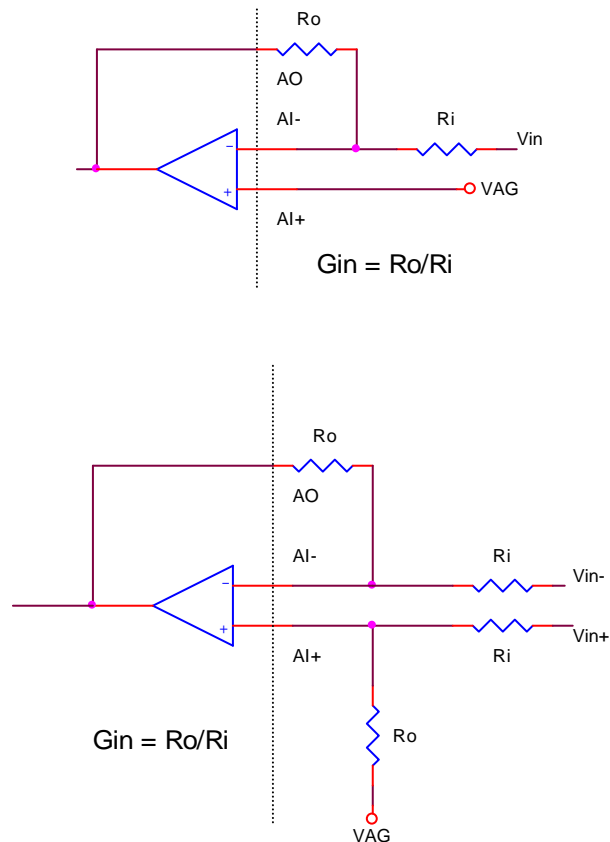
The 13-bit PCM code is a linear representation of the analog input. The MSB is the sign bit. The remaining 12 bits represent the absolute level. Because of the word length, the data rate must be greater than the regular telephony CODEC. With the telephony CODECs, the bit rate can be as low as 64 Kbps. This is because they are only sending 8 bits in the 125 μ seconds (8 KHz) sample window. Because the W681360 is sending more than 8 bits within the 125 μ seconds, the bit rate must be higher. In this particular design the minimum data rate is 256 Kbps.

The receive side of the W681360 has a special attenuator feature. Three additional bits are added onto the end of one 13-bit word. They control an attenuator in the receive path. These three bits provide eight different levels. These levels are in 3 dB steps from 0 to -21 dB. By including the 3-bit command with the PCM input, no additional pins are needed. The CODEC is signaled that the three additional bits are included in the word by taking the BCLKR pin HIGH (while the other clocks remain operating) for that frame. Then, using the BCLKT timing, the CODEC reads in the 14th, 15th, and 16th bits and adjusts the attenuation in the receive path according to the table in the data sheet. The following frames will then go back to the normal 13-bit mode. Now the analog output is set until the next time it needs to be changed. In an application, the processor would force the BCLKR pin HIGH for one frame. During this frame, it would insert the three bits onto the PCM input behind the other 13 bits. This could be done by several methods. One would be passing each byte through the processor, adding the three bits when needed. Another method would be to have the processor seize the line for the time of the three bits. The processor could have an open collector output tied to the PCM line just like the CODEC. The output would go active only during that short 3-bit time.

The Sign-Extended Mode is entered by holding the BCLKR pin LOW. Now the chip is both sending and receiving 16-bit PCM words. The first four bits are the sign bit now instead of just the first bit. (Although only a single sign bit is needed for the encoder/decoders the 16-bit data word is more easily processed in 16/32-bit DSP processors doing conferencing or echo-cancellation.) [The opposite method, not included on the W681360, is Zero-Extension when 3 zeros are added after the LSB.]

The W681360 has a resistor programmable gain stage on the analog input. This amplifier can be used either single-ended or in a differential mode. This is explained in Section 7.1 of the data sheet and in the below figure. The gain of the input stage should be calculated to result in a reference level (Zero Transmission Level Point) of 436 millivolts RMS or -5 dBm at 600 ohms. This level allows another +3.2 dB (headroom) for loud signals before the encoder begins to saturate or clip. For microphones, the amplifier gain can be as much as 30 dB. If high gain is selected, one must pay very careful attention to the PCB layout symmetry. Using the differential configuration will provide

better noise rejection than the single-ended mode. Section 7.1 also explains how the power amp can be powered up or down as needed. This results in a power savings during standby.

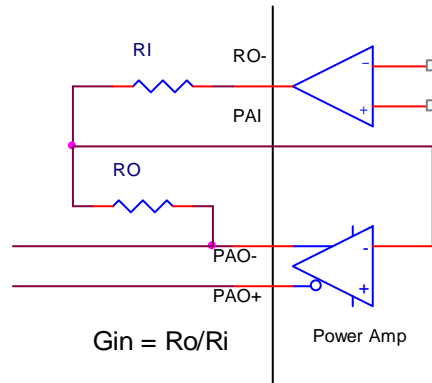


The W681360 has the ability to turn the input high-pass filter on or off. This allows the frequency response of the encoder to extend down to DC. This is controlled by the same pin that controls the A-Law or μ -Law selection of the telephony CODECs. For some applications, this is a desirable feature.

Otherwise, the pin configuration exactly matches that of the W681310 telephony CODEC. [In addition, the pin configuration exactly matches that of the MC145483 CODEC.] The linear, or companded, chips can be plugged into the same socket. That is, if the bit clock rate is 256 KHz or higher. The other end of the circuit must be changed, as well.

Finally, the CODEC has an adjustable power amplifier on the analog output side. It can drive a speaker, earphone or telephone line. This amplifier is also identical to the telephony CODEC, the W681310. The RO- output, which can drive a 2000 ohm load, can be applied through a gain setting resistor network, to provide higher drive for the various transducers. This differential amplifier can drive a 300 ohm load. Details on using this power amplifier are in Section 7.2 of the data sheet and

the below figure. Like the input amplifier, the power amplifier can be powered down to reduce current consumption during standby.



In conclusion, the W681360 Linear CODEC can be thought of as just another CODEC with a linear response and a few special features. It has the same pinout as the 8-bit telephony CODECs. This allows quick change of the encoding method without redesign of an application.

Important Notice

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